Test Resource Partitioning and Reduced Pin-Count Testing Based on Test Data Compression[1]

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Abstract

We present a new test resource partitioning (TRP) technique for reduced pin-count testing of system-on-a-chip (SOC). The proposed technique is based on test data compression and on-chip decompression. It makes effective use of frequency-directed run-length codes, internal scan chains, and boundary scan chains. The compression/decompression scheme decreases test data volume and the amount of data that has to be transported from the tester to the SOC. We show via analysis as well as through experiments that the proposed TRP scheme reduces testing time and allows the use of a slower tester with fewer I/O channels. Finally, we show that an uncompacted test set applied to an embedded core after on-chip decompression is likely to increase defect coverage.

1 Introduction

A system-on-a-chip (SOC) integrates several intellectual property (IP) cores. These cores must be tested using precomputed test sets provided by the core vendor. However, increased design complexity leads to higher test data volume for SOCs, which in turn leads to an increase in testing time [1]. One approach to reduce test time as well as overcome memory and I/O limitations of automatic test equipment (ATE), is based on test data compression and on-chip decompression [4–8]. Test data compression is especially appealing for SOCs with IP cores, for which BIST techniques based on gate-level structural knowledge are not feasible.

Test data compression is an example of a test resource partitioning (TRP) scheme for handling test complexity; see Figure 1. Test data volume and testing time are decreased by using a combination of coding techniques and faster on-chip decompression of encoded test data. The compressed data can be transferred at a slower rate from the ATE to the SOC. This allows the use of low-end ATEs with less memory and slower clock rates.

Reduced pin-count test (RPCT) is a well-known technique for reducing the number of integrated circuit (IC) pins that have to be contacted by the tester [2, 3]. RPCT requires full-scan design and boundary scan access to the chip I/Os. It enables testing of ICs using low-cost ATEs that have fewer functional pin channels than the number of IC I/O pins. The basic idea of RPCT is that only the clock pins, test control pins, scan-in and scan-out pins, and the TDI and TDO pins of the boundary scan chain are driven directly by the tester. The remaining functional pins are accessed through the boundary scan chain. RPCT helps in testing multiple sites simultaneously i.e., an ATE can test multiple chips in parallel. This can reduce test cost substantially, especially during wafer sort, when not all functional I/O pins are contacted. However, known RPCT schemes do not directly address the problem of test data volume.

We present a new TRP-based RPCT scheme that offers a number of important advantages. It leads to reduced testing time and test data volume, and it requires a smaller number of channels connecting the ATE to the SOC. The proposed scheme, which is based on frequency-directed run-length (FDR) codes for test data compression [8], allows us to readily overcome ATE memory and I/O bandwidth limitations. The reduction of test data was demonstrated in earlier work [8]. Here we concentrate on the test application time. We present detailed testing time analysis to demonstrate that a slower ATE can be used without impacting testing time. Such rigorous testing time analysis has not been presented earlier for test data compression schemes.

Yet another advantage of the proposed TRP-based RPCT scheme lies in the fact that it can potentially detect more defects than compacted test sets. Although compacted test sets for single stuck-at faults are widely used for testing, it is now recognized that they are not always effective for non-modeled faults and various defect types. In particular, since every modeled fault is now detected by fewer patterns, this approach can lead to reduced coverage of non-modeled faults [9, 10, 11]. It was shown in [10] that n-detection test sets, in which every fault is detected by at least n patterns ($n > 1$) and the average number of tests per fault is high, are more effective for detecting non-modeled faults. Since uncompacted tests are applied to the SOC after on-chip decompression, more detections per fault and therefore higher defect coverage is likely with the proposed TRP scheme.

The remainder of the paper is organized as follows. The test data compression and decompression architecture based

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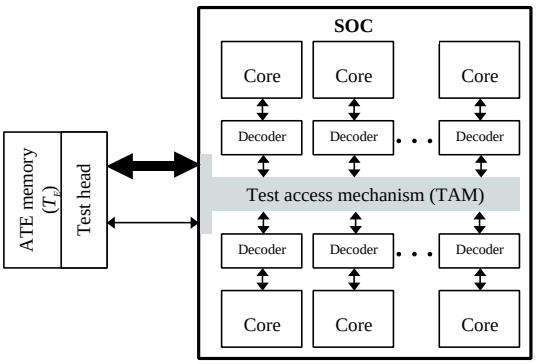

Figure 1. TRP scheme based on test data compression and on-chip decompression.

on FDR codes is reviewed in Section 2. We also present testing time analysis and the RPCT test architecture in Section 2. In Section 3, we show that test sets used for test data compression provide more n-detections and are therefore more likely to detect non-modeled faults than the uncompacted test sets. The experimental results are presented in Section 4, followed by conclusions in Section 5.

2 TRP using test data compression

We first review FDR coding and its application to test data compression [8]. The FDR code is a data compression code that maps variable-length runs of 0s to variable-length codewords. The FDR code is constructed as follows: The runs of 0s in the data stream are divided into groups $A_1, A_2, A_3, \ldots, A_k$, where k is determined by the length l_{max} of the longest run ($2^k - 3 \leq l_{max} \leq 2^{k+1} - 3$). Note also that a run of length l is mapped to group A_j where $j = \lceil \log_2(l+3) - 1 \rceil$. The size of the i^{th} group is equal to 2^i i.e., A_i contains 2^i members. Each codeword consists of two parts—a group prefix and a tail. The group prefix is used to identify the group to which the run belongs and the tail is used to identify the members within the group. The encoding procedure is illustrated in Figure 2. As an example, consider a run of five 0s ($r_1 = 000001$) in the input stream. Thus r_1 belongs to group A_2 and it is mapped to the codeword 1011. The reader is referred to [4, 8] for a detailed discussion and motivation for the FDR code.

An on-chip decoder decompresses the encoded test set T_E and produces the precomputed test set T_D. Even though T_D contains more patterns than the test sets obtained after static compaction of ATPG vectors, the testing time is reduced since pattern decompression can be carried out on-chip at higher clock frequencies. As discussed in [8], the decoder can be efficiently implemented by a k_{max}-bit counter, a $\log_2 k_{max}$-bit counter and a finite-state machine (FSM), where k_{max} is the maximum group size encountered during FDR coding of the test data stream. The synthesized decode FSM circuit contains only 4 flip-flops and 38 combinational gates. For any circuit whose test set is compressed using FDR code, the given logic is the only additional hardware required.

Group	Run-length	Group prefix	Tail	Codeword
A_1	0	0	0	00
	1		1	01
A_2	2	10	00	1000
	3		01	1001
	4		10	1010
	5		11	1011
A_3	6	110	000	110000
	7		001	110001
	8		010	110010
	9		011	110011
	10		100	110100
	11		101	110101
	12		110	110110
	13		111	110111
...	...	...	...	...

Figure 2. An example of FDR coding.

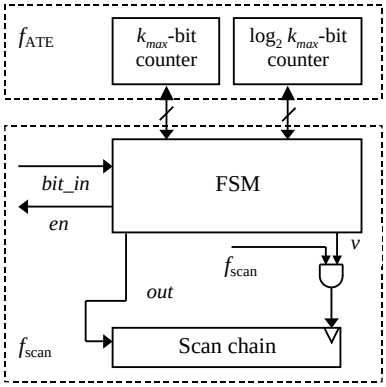

Figure 3. Block diagram of FDR decoder partitioned into two frequency domains for TRP.

Since the decoder for FDR coding needs to communicate with the tester, and both the codewords and the decompressed data can be of variable length, proper synchronization must be ensured through careful design. In particular, the decoder must communicate with the tester to signal the end of a block of variable-length decompressed data. These ATE requirements and other related decompression issues are discussed in detail in [6, 4].

2.1 Single scan chain

We first analyze the testing time when a single scan chain is fed by the FDR decoder. Test data compression decreases testing time, and allows the use of a low-cost ATE running at a lower frequency to test the core without imposing any penalties on the total testing time. Let the ATE frequency and the on-chip scan frequency be f_{ATE} and f_{scan}, respectively, where $f_{ATE} < f_{scan}$. Since the ATE and the scan chain operate at two different frequencies, the decoder also consists of two parts—one operating at f_{ATE} and the other operating at f_{scan} such that $f_{ATE} = f_{scan}/\alpha$, $\alpha > 1$. The parameter α should ideally be a power of 2 since it is easier to synchronize the ATE clock with the scan clock for such values of α [12]. If the scan chain has multiple segments

operating at different clock frequencies, each segment has a dedicated decoder for test data decompression.

Figure 3 outlines the decoder partitioned into two frequency domains. The proposed TRP scheme therefore decouples the internal scan chain(s) from the ATE via the use of a decoder interface. This decoupling implies that the scan clock frequency is no longer constrained by the ATE clock frequency limitation. Thus f_{scan} can now be made much larger than f_{ATE}.

For the FDR code, let $t(k,i)$ be the total time required to decompress a codeword that is the i^{th} member of the k^{th} group, and $t_{shift}(k,i)$ and $t_{decode}(k,i)$ be the time required to transfer the data from the ATE to the chip and to decode the codeword, respectively. An upper bound on $t_k(k,i)$ can be obtained by assuming that decoding begins after the complete codeword is transfered from the ATE. This implies that

$$t(k,i) \leq t_{shift}(k,i) + t_{decode}(k,i).$$

For FDR codes, the prefix length and the tail length of the codeword belonging to the k^{th} group is each equal to k; see Figure 2. Since data is transfered from the ATE to the chip at the tester frequency, the time required to transfer any codeword of the k^{th} group is given by

$$t_{shift}(k,i) = \frac{2k}{f_{ATE}}.$$

For run-length r_1 and $f_{ATE} = 20$ MHz, $k = 2$. Therefore, $t_{shift}(2,4) = 0.2\mu s$

For any codeword, the prefix is identical to the binary representation of the run-length corresponding to the group's first element. As shown in Figure 2, the number of 0s in the prefix of a codeword belonging to the k^{th} group is equal to $2^k - 2$. The decoder has to output $(2^k - 2)$ 0s before the tail decoding starts. The time $t_{prefix}(k)$ required to decompress the prefix of any codeword from the k^{th} group is therefore given by

$$t_{prefix}(k) = \frac{2^k - 2}{f_{scan}}.$$

The codeword for r_1 is 1011 and $k = 2$. Therefore, for $f_{scan} = 80$ MHz, $t_{prefix}(2) = 0.025\mu s$.

Similarly, the time $t_{tail}(k,i)$ required to decompress the tail of the i^{th} member of the k^{th} group is equal to the sum of time required to output $(i-1)$ 0s and a single 1. Hence,

$$t_{tail}(k,i) = \frac{(i-1)+1}{f_{scan}} = \frac{i}{f_{scan}}.$$

Run-length r_1 is the fourth member of group A_2. Therefore, $i = 4$ and $t_{tail}(2,4) = 0.05\mu s$.

The total decoding time $t_{decode}(k,i)$ is given by

$$\begin{aligned} t_{decode}(k,i) &= t_{prefix}(k) + t_{tail}(k,i) \\ &= \frac{2^k - 2}{f_{scan}} + \frac{i}{f_{scan}}. \end{aligned}$$

The total time needed to decompress the codeword is given by

$$\begin{aligned} t_k(k,i) &\leq t_{shift}(k,i) + t_{decode}(k,i) \\ &= \frac{2k}{f_{ATE}} + \frac{2^k - 2}{f_{scan}} + \frac{i}{f_{scan}} \\ &= \frac{1}{f_{ATE}}(2k + \frac{2^k - 2 + i}{\alpha}) \end{aligned} \quad (1)$$

where $f_{scan} = \alpha\ f_{ATE}$. The total decompression time for r_1 is given by $t_2(2,4) = 0.2\mu s + 0.025\mu s + 0.05\mu s = 0.275\mu s$.

Let $q(k,1), q(k,2), q(k,3), \ldots, q(k,2^k)$ be the absolute frequencies of the members of the k^{th} group. Therefore, the decompression time $\tau(k)$ for the runs belonging to k^{th} group is given by

$$\begin{aligned} \tau(k) &= \frac{1}{f_{ATE}} \sum_{i=1}^{2^k} (2k + \frac{2^k - 2 + i}{\alpha}) q(k,i) \\ &= \frac{1}{f_{ATE}} (2k \sum_{i=1}^{2^k} q(k,i) + \frac{1}{\alpha} \sum_{i=1}^{2^k} (2^k - 2 + i) q(k,i)). \end{aligned}$$

Let us assume that k_{max} is the largest group. The test application time TAT_{SSC} for the entire test set with a single scan chain (SSC) is given by

$$\begin{aligned} TAT_{SSC} &\leq \sum_{k=1}^{k_{max}} \tau(k) \\ &= \frac{1}{f_{ATE}} (|T_E| + \frac{1}{\alpha} \sum_{k=1}^{k_{max}} \sum_{i=1}^{2^k} (2^k - 2 + i) q(k,i)) \end{aligned}$$

where $|T_E|$ is the size of the encoded test set. Next, to derive a lower bound on the testing time, suppose the tail bits are shifted in while the prefix is being decompressed. Since, the tail bits are now shifted in parallel while the prefix bits are decoded, a lower bound on decoding time using (1) is given by:

$$\begin{aligned} t(k,i) &\geq \frac{k}{f_{ATE}} + \frac{2^k - 2}{f_{scan}} + \frac{i}{f_{scan}} \\ &= \frac{1}{f_{ATE}} (k + \frac{2^k - 2 + i}{\alpha}) \end{aligned}$$

Therefore,

$$TAT_{SSC} \geq \frac{1}{f_{ATE}} (\frac{|T_E|}{2} + \frac{1}{\alpha} \sum_{k=1}^{k_{max}} \sum_{i=1}^{2^k} (2^k - 2 + i) q(k,i)).$$

We next compare the testing time using the proposed TRP scheme with that for an ATPG-compacted test set with p patterns and an external tester operating at frequency $f^{\star}_{ATE}$. Let the length of the scan chain be n bits. The size of the ATPG-compacted test set is pn bits and the test application time TAT^{ATPG}_{SSC} equals $pn/f^{\star}_{ATE}$. We now derive the ratio $\gamma = f^{\star}_{ATE}/f_{ATE}$ such that $TAT^{ATPG}_{SSC} = TAT_{SSC}$.

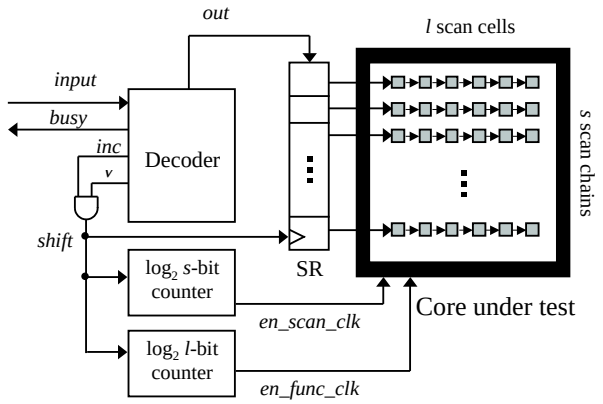

Figure 4. Decompression architecture for a CUT with multiple scan chains.

An upper and a lower bound on γ can be derived using the upper and lower bound values of TAT_{SSC}. Therefore,

$$\frac{pn}{|T_E| + \frac{1}{\alpha}\sum_{k=1}^{k_{max}}\sum_{i=1}^{2^k}(2^k - 2 + i)q(k,i)} \geq \gamma \geq \frac{pn}{\frac{|T_E|}{2} + \frac{1}{\alpha}\sum_{k=1}^{k_{max}}\sum_{i=1}^{2^k}(2^k - 2 + i)q(k,i)}.$$

Experimental results presented in Section 5 show that the testing time is reduced considerably using the proposed method if $f^{\star}_{ATE} = f_{ATE}$. Moreover, if the same testing time is desired using a slower ATE ($f^{\star}_{ATE} > f_{ATE}$), the ratio γ is especially high for larger values of α. Hence FDR coding allows us to decrease the volume of test data and use a slower tester without increasing testing time.

To conclude the analysis, we note that the above bounds allow us to evaluate the testing time without a detailed analysis of the asynchronous handshaking protocol between the tester and the decoder. The exact testing time, which lies between the two bounds can be determined through a bit-by-bit analysis of the encoded test data. The formulation based on upper and lower bounds allows us to demonstrate the effectiveness of the proposed TRP scheme without resorting to such detailed analysis.

2.2 Multiple scan chains

Let us consider a core under test with s scan chains, each of length l; see Figure 4. A shift register SR is used to serially shift data from the decoder and then load the scan chain in parallel (SR can be configured out of the first scan cell of each scan chain.). Two counters are used to indicate that SR and the scan chains are loaded. The counter used for SR and the scan chains are $\log_2 s$ bits and $\log_2 l$ bits long, respectively. SR is loaded with a new bit only when the decoder output is valid and $\log_2 s$ bit counter is incremented for every valid bit. When SR is fully loaded, scan clock is enabled to shift the data from SR to the scan chains. For every bit loaded into the scan chains, the $\log_2 l$ bit counter

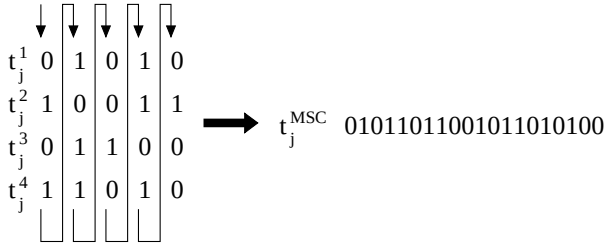

Figure 5. Generating the interleaved data stream for a circuit with four scan chains.

is incremented. When the scan chain is completely loaded, the functional clock is enabled to apply the pattern to the core.

The test set has to be reorganized for the above test architecture before applying test data compression. Let the test pattern j for i^{th} scan chain be $t^i_j = b^i_{j1}b^i_{j2}b^i_{j3}\ldots b^i_{jl}$, where b^i_{jk} is the k^{th} bit of the j^{th} pattern and the i^{th} scan chain. Let t^{MSC}_j be the j^{th} pattern of the modified test set for a core with multiple scan chains (MSC). Therefore, t^{MSC}_j is obtained by forming a single stream of bits by interleaving the bits of the j^{th} pattern of each scan chain i.e., $t^{MSC}_j = b^1_{j1}b^2_{j1}b^3_{j1}\ldots b^l_{j1}, b^1_{j2}b^2_{j2}b^3_{j2}\ldots b^l_{j2}, \ldots, b^1_{jl}b^2_{jl}b^3_{jl}\ldots b^l_{jl}$. Figure 5 illustrates the procedure of obtaining the new test pattern for four scan chains. The testing time analysis of Section 2.1 can now be directly applied to the FDR coding of the modified test data sequence.

2.3 RPCT based on test data compression

RPCT is effective for designs with a small number of scan pins [2]. However, IC designs often incorporate multiple-scan chains to reduce testing time. For such designs, RPCT needs to contact all the scan pins and therefore does not provide any advantage. The enhanced reduced pin-count test (E-RPCT) technique provides a solution to the above problem by loading multiple-scan chains in parallel through the boundary scan chain [3]. The boundary scan chain is divided into multiple segments and these segments are used to carry out the serial to parallel conversion while loading the scan chains. Although E-RPCT helps in reducing testing time for cores with multiple-scan chains, it does not address the problem of test data volume as it requires large tester memory for the pins to be contacted. A promising solution is to combine E-RPCT with the proposed TRP scheme.

RPCT based on test data compression is shown in Figure 6. The external tester feeds the encoded test data T_E through the TDI and the scan-in pins. T_E is decompressed on-chip using the decoder and the test patterns are loaded into the boundary-scan chain. The boundary-scan chain is then used to load the internal scan chains in parallel. The boundary-scan chain is divided into multiple segments to shift-in the test data serially from the decoder. When the boundary-scan chain is completely loaded, data is trans-

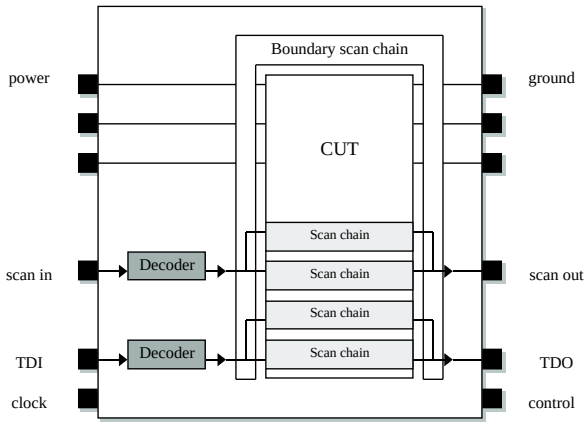

Figure 6. RPCT based on test data compression.

fered to the internal scan chains in parallel. Similarly, the boundary-scan chain is used to load the data to the primary inputs of the core. The test responses are captured in the internal scan chains and the boundary-scan chain and shifted out through the scan-out and TDO pins. The proposed RPCT scheme helps in reducing the test data volume since the ATE stores the small encoded test set. The testing time is reduced as multiple chips can be tested in parallel using RPCT and also because the decoding is done on-chip at a higher clock frequency. The proposed scheme enables the use of low-cost ATEs, thus bringing down the total test cost. Since the scheme uses the boundary-scan chain, which is $IEEE$ 1149.1 compliant, it can be used for carrying out various other tests.

3 Enhanced defect coverage

It has recently been shown that n-detection test sets, in which every fault is detected by n ($n > 1$) tests, are more effective in detecting defects that are not modeled by stuck-at faults [9, 10, 11]. In this section, we show that the uncompacted test sets that are applied to the core under test after decompression provide a higher degree of n-detection than ATPG-compacted test sets. This in itself is not surprising since a large number of patterns are now being applied to the core under test. However, when viewed in the context of reduced data volume and testing time, greater n-detection (and potentially higher defect coverage) emerges as an important benefit of the proposed TRP scheme. Note that there is no loss in the coverage of modeled faults due to test data compression.

In order to determine the number of times a fault is detected by an uncompacted test sets, we used the FSIM fault simulator [14] and test cubes generated using the Mintest ATPG program [13]. The test cubes were encoded using FDR coding, and the resulting decompressed patterns were applied to the larger ISCAS-89 benchmark circuits. Since random-testable faults are usually detected by a large number of patterns, we only considered random-pattern resistant faults, which were left undetected after the application of 1024 patterns, and tabulated the number of detections for each such fault. As a baseline case, we repeated the experiments for the Mintest-compacted patterns.

Circuit	f_{ATE} (MHz)	α	Lower bound on TAT_{SSC} (ms)	Upper bound on TAT_{SSC} (ms)	TAT_{SSC}^{ATPG} (ms)
s5378	20	4	0.526	0.756	1.037
		8	0.378	0.607	1.037
		16	0.303	0.533	1.037
s9234	20	4	0.877	1.263	1.296
		8	0.631	1.018	1.296
		16	0.509	0.895	1.296
s13207	20	4	2.574	3.083	8.155
		8	1.541	2.050	8.155
		16	1.025	1.534	8.155
s15850	20	4	1.502	2.041	2.871
		8	1.020	1.560	2.871
		16	0.780	1.320	2.871
s38417	20	4	3.485	4.912	5.657
		8	2.456	3.882	5.657
		16	1.941	3.368	5.657
s38584	20	4	4.247	6.005	8.052
		8	3.002	6.005	8.052
		16	2.380	4.138	8.052

Table 1. Comparison of testing time using the proposed TRP method with traditional scan-based external testing.

Experimental results presented in Section 4 show that for $n > 1$, the number of detections is significantly higher for the proposed TRP scheme. Thus increased defect coverage appears to be an added benefit of test data compression and on-chip decompression scheme.

4 Experimental results

In this section, we present experimental results on the testing time for the TRP scheme based on FDR coding. The effectiveness of FDR coding for test data volume reduction was shown in [8]; these results are therefore not presented here. We also determine the percentage of single stuck-at faults that are detected multiple times, both for uncompacted and compacted test sets for the large ISCAS-89 benchmark circuits. The test sets were obtained using the Mintest ATPG program, which is known to yield the most compact test sets for the benchmark circuits.

Table 1 presents test application time for the proposed method and for traditional scan-based testing with $f_{ATE}^{\star} = f_{ATE}$. We note that in all the cases the upper bound on test application time using the proposed scheme is lower than that for scan-based external testing. The actual test application time for the proposed TRP scheme lies between the lower and upper bounds. For example, the test application time for s38584 with $\alpha = 8$, and $f_{ATE}^{\star} = f_{ATE} = 20$ MHz lies between 3.002 ms and 6.005 ms, which is lower than the time of 8.052 ms required for external testing.

Table 2 shows lower and upper bounds on $\gamma = f_{ATE}^{\star}/f_{ATE}$. Recall that we are attempting to use a slower ATE with frequency f_{ATE}, yet have the same testing time as that for a faster ATE with frequency $f_{ATE}^{\star}$, which applies

Circuit	$(\gamma_{\min}, \gamma_{\max})$		
	$\alpha = 4$	$\alpha = 8$	$\alpha = 16$
s5378	(1.37,1.97)	(1.70,2.74)	(1.94,3.41)
s9234	(1.02,1.47)	(1.27,2.05)	(1.44,2.54)
s13207	(2.64,3.16)	(3.97,5.28)	(5.31,7.95)
s15850	(1.46,1.91)	(1.88,2.81)	(2.2,3.68)
s38417	(1.15,1.62)	(1.45,2.30)	(1.67,2.91)
s38584	(1.34,1.89)	(1.69,2.68)	(1.94,3.38)

Table 2. Lower and upper bounds on $\gamma = f^{\star}_{ATE}/f_{ATE}$.

Circuit	**Percentage of faults detected more than once**	
	Compacted test set	Uncompacted test set
s9234	52.09	61.31
s13207	35.33	48.75
s15850	46.77	65.66
s38417	51.78	56.79
s38584	44.18	51.53

Table 3. The number of detections for compacted and uncompacted test sets.

compacted test patterns to the core under test. We assume a single scan chain for each of the benchmark circuits, and use the analytical results of Section 2.1. The bounds on γ are listed for various values of α, the ratio between the on-chip frequency f_{scan} and f_{ATE}. For example, if $\alpha = 8$ for the benchmark s13207, i.e. $f_{scan}/f_{ATE} = 8$, and the same testing time is desired for the two methods, we need an ATE that runs between 3.97 and 5.28 faster than the ATE required with the TRP scheme. In other words, if $f_{scan} = 200$ MHz and $f_{ATE} = 25$ MHz, a faster ATE that runs at a frequency between 99 MHz and 132 MHz will be needed if the TRP scheme is not used.

Table 3 compares the number of fault detections for the compacted and the uncompacted test sets. Table 3 shows that for the large ISCAS-89 benchmark circuits, the number of faults that are detected more than once is much higher for the uncompacted test set. Table 4 shows the average number of detections (tests) n_{av} for each fault. We find that the value of n_{av} for uncompacted test sets is much higher than for compacted test sets. A test set with higher n-detection and n_{av} value is more likely to detect more non-modeled faults and provide high defect coverage. Therefore, TRP using test data compression/decompression not only reduces test data volume and testing time but it is also likely to provide increased defect coverage.

5 Conclusions

We have shown that test data compression can be used for effective test resource partitioning and reduced pin-count testing. The on-chip decompression of test pattern decouples the internal scan chain(s) from the ATE, thereby allowing higher scan clock frequency. We have presented a rigorous testing time analysis for compression/decompression based on FDR codes. Experimental results for the ISCAS-89 benchmark circuits show that a slower ATE can often be used with no adverse impact on testing time. Therefore, the proposed approach not only decreases test data volume and the amount of data that must be transfered from the ATE, but it also reduces testing time and facilitates the use of less expensive ATEs. Finally, an added benefit of the proposed TRP technique is that it is likely to increase defect coverage since it increases the degree of multiple detections for modeled faults.

Circuit	**Average number of tests per fault**	
	Compacted test set	Uncompacted test set
s9234	3.30	5.15
s13207	2.89	6.00
s15850	2.49	6.05
s38417	6.04	6.48
s38584	2.28	5.60

Table 4. Average detection values, n_{av} for compacted and uncompacted test sets.

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