Automatic Generation of Common-Centroid Capacitor Arrays with Arbitrary Capacitor Ratio

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Abstract

The key performance of many analog circuits is directly related to accurate capacitor ratios. It is well known that capacitor ratio precision is greatly enhanced by paralleling identical size unit capacitors in a common-centroid geometry. In this paper, a general algorithm for fitting arbitrary capacitor ratios in a common-centroid unit-capacitor array is presented. The algorithm gives special care to both non-integer and identical ratios in order to minimize mismatch. A method for capacitance mismatch estimation based upon an oxide gradient model is also introduced. It enables the comparison of different unit-capacitor array assignments. Layout issues are discussed with emphasis on a generic routing model. Both the algorithm and the mismatch estimation method are implemented in an automatic capacitor array generation tool.

1. Introduction

One of the important issues during the layout phase of some types of A/D, D/A converters [1] and filters is the achievement of precise capacitor ratios. Key performance in most cases depends on capacitor ratios rather than absolute capacitance. However, this requires complicated and time-consuming full-custom layout. Even for the emerging automatic analog layout generation tools [2, 3] special sophisticated module generators, that include relevant layout techniques, seem to be indispensable.

Capacitor mismatch can be attributed to two sources of errors: random and systematic [4]. Random error mechanisms include both random edge and oxide effects. Random errors set a minimum limit on the unit capacitance value for a given accuracy. Also, for a typical CMOS process, global effects dominate [4]. Common-centroid geometries are thus particularly important to reduce this type of errors.

On the other hand, systematic mismatch is that part of the total mismatch where a deterministic trend can be observed in the mismatch values of various capacitors. Five sources of systematic mismatch have been identified and studied in [5]. Based on this, a list of generic layout rules was developed. Process gradients, for example gradients in oxide thickness, contribute to systematic mismatch. The direction of the gradient is a function of the die location on the wafer [6]. Gradients are generally assumed to be represented by a linear function [1, 7]. Again common-controid capacitor arrangement helps to cancel this kind of error.

Most of the published work on capacitance mismatch, though very limited, is only concerned with the modeling of different sources of error. Even though it is well known that the best way to achieve acceptable matching between multiple capacitors with arbitrary capacitance ratios is through unit capacitors placed in a common-centroid capacitor array to form larger capacitors [1], this process is still done following a case-by-case approach.

Few trials can be found in the literature, which aim to automate this error-prone and laborious process. In [8], assignment of unit capacitors is performed under two basic constraints: At least one neighbor of each unit is another unit of the same capacitor, in the same time each capacitor must have at least one unit on either side of the array. While this method results in a compact array for arbitrary ratios, common-centroid placement is not considered at all. In [9], common-centroid placement, symmetrical routing and parasitic balance are considered through a special optimization algorithm. However, it is only restricted to device pairs.

In this paper, a general algorithm for unit-capacitor assignment of arbitrary capacitor ratios is introduced with emphasis on non-integer and identical ratios. Being systematic, the algorithm is suitable to be implemented in a dedicated capacitor array device generator and integrated in automatic layout tools. In order to *quantify* the mismatch due to oxide gradients, a method that allows both the estimation of the mismatch due to oxide gradients and the comparison of various array cell assignment, is presented. Finally, comparison with a previous published result [8] is given.

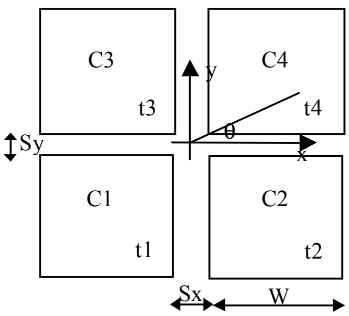

Figure 1. Mismatch estimation

2. Mismatch estimation

For a group of capacitors with arbitrary ratio, the *ratio mismatch* is calculated for each pair of capacitors and the largest value is retained. For N_{cap} capacitors with capacitance ratio $R_1:R_2:\ldots:R_{Ncap}$, which after the parallel unit-capacitor layout becomes $R_1^*:R_2^*:\ldots:R_{Ncap}^*$, we define the capacitance ratio mismatch M by:

$$M = \max\left(\left|\frac{\frac{R_i^*}{R_j^*}-\frac{R_i}{R_j}}{\frac{R_i}{R_j}}\right|\right)\times 100 = \max\left(\left|\frac{R_i^*}{R_j^*}\frac{R_j}{R_i}-1\right|\right)\times 100\,\% \quad (1)$$

for all i and j. This means that mismatch is always positive.

If we further assume that mismatch is dominated by oxide gradients, using a *simple integral model* similar to that used for transistors in [10], the equivalent oxide thickness of each capacitor is defined as:

$$t_{eq} = \frac{\iint\limits_{Capacitor\ Area} t(x,y)\,dx\,dy}{Capacitor\ Area} \quad (2)$$

where the capacitor area is the total area of all parallel capacitors making-up each capacitor.

A more accurate approach presented in [7] as a *segmented integral model*, is followed. In this case, each capacitance is modeled as the parallel connection of *lumped* unit-capacitors. Equation (2) is then used independently to obtain the equivalent oxide thickness of each unit-capacitor component.

For example, Fig. 1 shows four capacitors C1, C2, C3 and C4 with a linear oxide gradient α in the direction specified by the angle θ. If we consider that they are grouped to form two capacitors Ca=C1+C4 and Cb=C2+C3 such that Ca:Cb=1:1, according to (1)

$$M_{Ca-Cb} = \max\left(\left|\frac{C1+C4}{C2+C3}-1\right|, \left|\frac{C2+C3}{C1+C4}-1\right|\right)\times 100\,\% \quad (3)$$

Since both Ca and Cb share a common-centroid located at the center of the capacitor array, using the simple integral

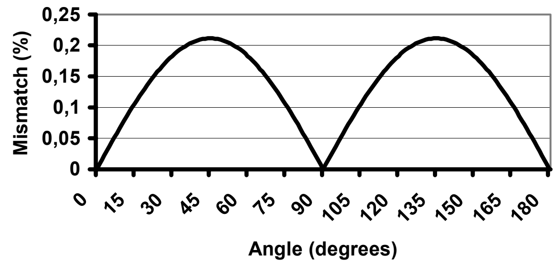

Figure 2. Mismatch variation with gradient angle

model [10] will render $t_{eq-Ca} = t_{eq-Cb} = t0$, where $t0$ is the oxide thickness at the origin, which gives Ca=Cb. But the segmented integral model [7] gives

$$t1 = t0 - \alpha\frac{1}{2}(Sx+W)\cos\theta - \alpha\frac{1}{2}(Sy+W)\sin\theta \quad (4)$$

$$t2 = t0 + \alpha\frac{1}{2}(Sx+W)\cos\theta - \alpha\frac{1}{2}(Sy+W)\sin\theta \quad (5)$$

$$t3 = t0 - \alpha\frac{1}{2}(Sx+W)\cos\theta + \alpha\frac{1}{2}(Sy+W)\sin\theta \quad (6)$$

$$t4 = t0 + \alpha\frac{1}{2}(Sx+W)\cos\theta + \alpha\frac{1}{2}(Sy+W)\sin\theta \quad (7)$$

Therefore,

$$Ca = C1 + C4 = \varepsilon A\left(\frac{1}{t1}+\frac{1}{t4}\right) = C0\left(\frac{1}{t1/t0}+\frac{1}{t4/t0}\right) \quad (8)$$

and

$$Cb = C2 + C3 = \varepsilon A\left(\frac{1}{t2}+\frac{1}{t3}\right) = C0\left(\frac{1}{t2/t0}+\frac{1}{t3/t0}\right) \quad (9)$$

It is clear that the mismatch ≠ 0 only for a first order approximation.

Consider the above array with a unit capacitor side (W) of 25µm, an oxide thickness ($t0$) of 40nm, an oxide gradient (α) of 100ppm, a vertical and horizontal spacing (Sx and Sy) of 1µm. Mismatch variation with the gradient angle (θ) is calculated and shown in Fig. 2. It is apparent that for angles of 0°, 90° and 180° mismatch due to the oxide gradient reaches zero, while it is maximum at 45° and 135°. We are often concerned with maximum mismatch since the gradient angle can't be predicted [6].

3. Algorithm

In this section the proposed systematic algorithm for unit-capacitor assignment is presented. The inputs are:

- The number of matched capacitors N_{cap}
- The capacitance ratio $R_1:R_2:\ldots:R_{Ncap}$
- The unit capacitance C_u, such that $C_1=C_uR_1$, …
- A layout shape factor: aspect ratio, …
- Layout design rules: minimum width and spacing, …

Layout generation proceeds in the following steps:

1. Determination of rows (N_r) and columns (N_c)
2. Assignment of unit capacitors to the array cells
3. Mismatch estimation
4. Layout generation

Each of these steps is described below in more details.

3.1. Array dimensions ($N_r \times N_c$)

All unit capacitors are assumed to be square-shaped with a side dimension of W µm, which is determined according to the given C_u and process specific capacitance. Based on the given layout factor, the unit capacitor side dimension W, the spacing between adjacent unit capacitors both in the x- and y-directions (S_x and S_y), and the total number of unit capacitors N_u given by:

$$N_u = \sum_{i=1}^{i=N_c} \text{round\_to\_greater\_integer}(R_i) \qquad (10)$$

N_r and N_c are calculated.

3.2. Cell assignment

In this step, the units of all capacitors are assigned to specific cells in the generated array. In order to achieve common-centroid placement, we studied possible forms of capacitance ratios and the available geometrical structures in rectangular arrays suitable to each case.

Capacitor ratios: They are classified into:

- Even unit-capacitor ratios.
- Odd unit-capacitor ratios.
- Non-integer ratios: Theses are non-integer ratios of the form $i\frac{x}{y}$, where i is an integer and $\frac{x}{y}$ is a ratio less than one. Special layout techniques exist to realize a non-integer value of unit-capacitors that preserves the same area-to-perimeter ratio. For example, i-1 capacitors are realized using unit square cells, while the last non-unit capacitor is a rectangular-shaped capacitor with a *hole* to control the capacitor perimeter [11], this technique is adopted since it requires only two adjacent cells.
- Identical ratios: These are ratios that occur more than once in the capacitor array. They require a special care in cell assignment, since they need to be assigned in exactly the same way for maximum matching.

Geometrical structures: By inspection of the rectangular array, the geometrical following structures are observed:

- Circles: A circle is composed of cells having the same distance from the center of the array. Fig. 3(a) shows an array example with its available circles. Cells are placed in groups of circles according to their distance from the center. There are also an order of cells inside each circle, the basic idea is that each two consecutive pair of cells are in a diagonal symmetry with respect to the array center as shown by the arrows in Fig. 3(a).

5	4	3	4	5
4	2	1	2	4
3	1	0	1	3
4	2	1	2	4
5	4	3	4	5

(a)

1	1	1	1	1
1	2	2	2	1
1	2	3	2	1
1	2	2	2	1
1	1	1	1	1

(b)

Figure 3. (a) Circles and (b) rectangles.

- Rectangles: A rectangle is composed of cells on the same rectangle parallel to the outer array rectangle. Fig. 3(b) shows an array example with its available rectangles. In order to construct these rectangles, cells in the outer rectangle of the array are scanned, followed by the inner rectangle and so on. Note that rectangles are composed of one or more circles. The order of cells inside each rectangle starts from the upper left corner and proceeds as shown by the arrows on Fig. 3(b).

Cell assignment: Depending on ratio types mentioned above, assignment is done as follows:

- Even ratios: From the symmetrical nature of the two-dimensional array, it is obvious that even ratios can be easily assigned respecting the common-centroid constraint. They are placed in the *circles* as follows:
    1. For each even ratio, and starting from the innermost circle, circles with the number of cells that sum up to exactly the required even ratio are chosen.
    2. If circles with the *exact* sum cannot be found in the set of available circles, only the smallest available circle is filled. This ratio is then abandoned.
    3. The following even capacitance ratios are similarly treated.
    4. The above process is then repeated till all even ratios are assigned. This allows maximum interdigitation between capacitors.
- Odd ratios: Due to the rectangular nature of the array, odd ratios create an inherent asymmetry. Only one cell is taken from each odd ratio and placed in the smallest available circle(s) to decrease the deviation of their centroids from the array center. This leaves only even ratios that are placed as described above.
- Non-integer ratios: The total number of required cells is determined, and the ratio is treated either as an odd or even one as described above. One additional constraint, however, exists for non-integer ratios: assigned cells (*in circles*) must include two adjacent cells for the rectangular-shaped non-unit capacitor. Routing channels are either horizontal or vertical. This means that the non-unit rectangular capacitor should be in the same direction as that of the routing channels. In order to achieve this condition during non-integer ratio assignment, after the

H4	G4	F1	G1	H1
F6	D4	C1	D1	F3
E4	B4	A1	B1	E1
E2	B2	A2	B3	E3
F4	D2	C2	D3	F5
H2	G2	F2	G3	H3

(a) Circles

3	4	5	3	4
5	2	5	2	5
4	2	1	3	3
3	4	1	2	4
5	2	5	2	5
4	3	5	4	3

(b) Cell assignment

Figure 4. Assignment of a 1.2:5.8:7:7:8 ratio

first circle is assigned, if no adjacent cells in the required direction are found, an adjacent cell is directly assigned together with its diagonally opposite cell.

- Identical ratios: They are placed in *rectangles*:
  1. Starting from the innermost rectangle, rectangle(s) with the number of cells that sum up to exactly the number of all unit-capacitors of identical ratios are reserved.
  2. If rectangle(s) with the *exact* sum can not be found in the set of available rectangles, larger rectangle(s) are selected and empty cells are left free such that they are spaced equidistantly on the rectangle (in fact, empty cells are chosen on *circles*).
  3. One cell is placed alternatively from each identical ratio on the rectangle. This guarantees that they are placed identically with maximum interdigitation.

It is to be noted that for the special case of a capacitor array with only two capacitors of identical unit-capacitor ratios, this results in the well-known chessboard-like unit-capacitor distribution.

Assignment priority: During cell assignment priority is given to the most critical cases as follows:

1. Ratios less than two, since they may need two adjacent cells and must be placed nearest to the center.
2. One cell from each odd ratio (placed in the innermost *circles*), the remaining ratios thus become all even ones.
3. Identical ratios (in *rectangles*).
4. Non-integer ratios (in *circles* with at least two adjacent cells) and the remaining even ratios (in *circles*) placed alternatively in one circle per ratio.

In addition, within each of the above categories, ratios are ordered from smaller (higher priority) to larger ratios.

Example: Consider five capacitors of unit-capacitance ratios given by R_1:R_2:R_3:R_4:R_5 = 1.2:5.8:7:7:8, using equation (10) we find that the total number of required cells (N_u) is 30. Fig. 4(a) shows a 6×5 array. The letter inside each cell indicates *circles*. The array contains 8 circles grouped in an ascending order (from A to H) according to their radius, where the center is located at the middle of the array. The number next to each letter defines the order of cell assignment inside each circle shown by the arrows on Fig. 3(a). The ratios contain 3

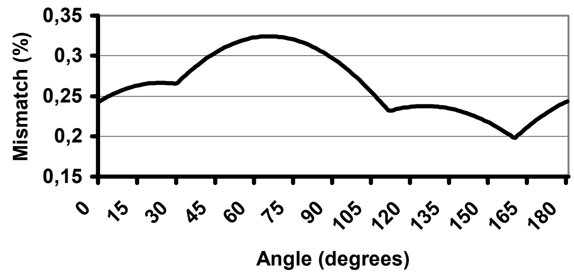

Figure 5. Mismatch with gradient angle of Fig. 4

even ratios (R_1, R_2 and R_5), 2 odd ratios (R_3 and R_4), 2 non-integer ratios (R_1 and R_2), 2 identical ratios (R_3 and R_4) and one ratio less than 2 (R_1).

According to cell assignment priority, cell assignment proceeds as follows, refer to Fig. 4(b):

1. R_1 is placed in the smallest circle A.
2. Only one unit from each odd ratio (R_3 and R_4) is placed in the following circle cells B1 and B2.
3. The sum of cells of identical ratios R_3 and R_4, which becomes even after the last step, is 12. The only rectangle that can hold such number of cells is the outer one. Since its number of cells (18) is greater than the needed sum, a circle whose cells are exactly the difference is excluded (circle F). R_3 and R_4 are placed alternatively on the remaining cells of the rectangle.
4. Non-integer and even ratios are then treated, namely R_2 and R_5. R_2 occupies the rest of circle B, but since no adjacent cells are found, an appropriate adjacent cell is directly assigned (cell D3) together with its diagonally opposite one (cell D4). We then proceed alternatively between ratios R_5 and R_2 as follows: the next circle C is assigned to R_5, the following circle D (or its remaining cells) is assigned to R_2, and finally the last empty circle F is assigned to R_5.

3.3. Mismatch estimation

Fig. 5 shows mismatch calculations based on equation (1), with W=25µm, $t0$=40nm, α=10ppm. Routing channels are vertical such that Sx and Sy are 9.1 and 2.6µm respectively in a 0.35-µm process.

3.4. Layout generation

Fig. 6 shows the layout corresponding to the capacitor array given in Fig. 4. Routing channels are chosen either horizontally or vertically in order to minimize the routing area and reduce cross-coupling capacitance. Routing channels of top plates are separated from those of the bottom plates to avoid additional coupling capacitance that alters the value of the original capacitors. Dummy capacitors surround the array. Interconnect lines extend on both sides of unit capacitors to reduce errors due to

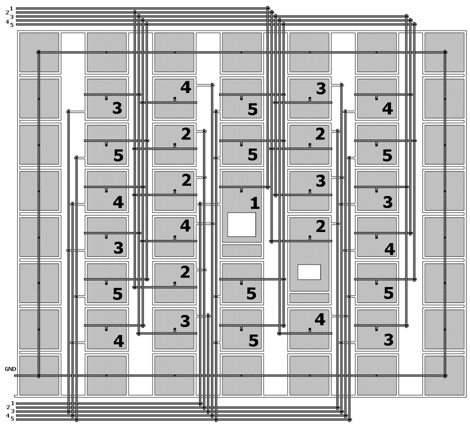

Figure 6. Layout of the array shown in Fig. 4

mask misalignment. Holes inside capacitors are added to realize non-unit ratios while keeping constant area-to-perimeter ratio [11]. Routing depends on cell assignment. However, routing lines increase with the number of unit-capacitors so the added capacitance is approximately ratioed. It should be noted that the rules given in [5] were also respected.

4. Comparison

The proposed algorithm is compared to that published in [8] and shown in Fig. 7(a) for five capacitors of unit-ratio 1:1.4:2:9.2:17. Both algorithms are capable of treating arbitrary capacitor ratios. In [8], priority has been given to minimizing the overall area, while in our case mismatch minimization is the first concern. Using the presented algorithm, constructed circles are shown in Fig. 7(b), while assigned unit-capacitors are shown in Fig. 7(c). Mismatch calculations for both cases are shown in Fig. 8. It is apparent that mismatch due to oxide gradients is reduced by an order of magnitude in our case.

1	3	3	5
5	5	5	5
5	5	5	5
5	5	5	5
5	4	4	4
5	4	4	4
5	2	4	4
5	2	4	4

(a) array in [8]

G	F	F	G
E	D	D	E
C	B	B	C
B	A	A	B
B	A	A	B
C	B	B	C
E	D	D	E
G	F	F	G

(b) Circles

5	5	5	5
5	4	4	5
5	4	3	5
4	1	2	4
4	5	2	4
5	3	4	5
5	4	4	5
5	5	5	5

(c) This work

Figure 7. Comparison between [8] and this work

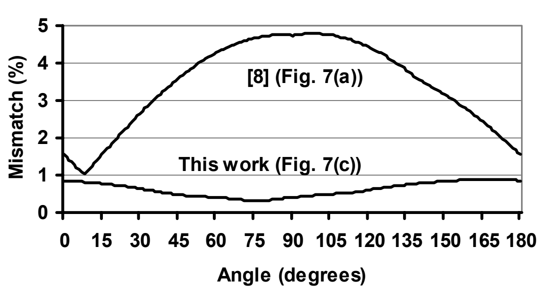

Figure 8. Mismatch with gradient angle θ for Fig. 7

5. Conclusions

In this paper, common-centroid placement of arbitrary capacitor ratios is studied. This has resulted in a general algorithm for unit-capacitor assignment in rectangular arrays. Being systematic the algorithm is suitable for CAD implementations. A method for mismatch estimation is proposed and used to compare different cell assignment techniques. A module generator for capacitor arrays is developed. It produces the layout of arbitrary capacitor ratios based on the above algorithm and mismatch calculations.

References

[1] J. L. McCreary and P. R. Gray. All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques – Part I. *IEEE J. of Solid-State Circuits*, 10(6):371-379, Dec. 1975.
[2] K. Lampaert, G. Gielen and W. M. Sansen. Performance-Driven Placement Tool for Analog Integrated Circuits. *IEEE J. of Solid-State Circuits*, 30(7):773-780, Jul. 1995.
[3] J. M. Cohn and R. A. Rutenbar and L. R. Carley. KOAN/ANAGRAM II: New Tools for Device-Level Analog Placement and Routing. *IEEE J. of Solid-State Circuits*, 26(3):330-342, Mar. 1991.
[4] J.-B. Shyu, G. C. Temes and F. Krummenacher. Random Error Effects in Matched MOS Capacitors and Current Sources. *IEEE J. of Solid-State Circuits*, 19(6):948-955, Dec. 1984.
[5] M. J. McNutt, S. LeMarquis and J. L. Dunkley. Systematic Capacitance Matching Errors and Corrective Layout Procedures. *IEEE J. of Solid-State Circuits*, 29(5):611-616, May 1994.
[6] E. Felt, A. Narayan and A. Sangiovanni-Vincentelli. Measurement and Modeling of MOS Transistor Current Mismatch in Analog IC's. In *Proc. ACM*, pages 272-277, 1994.
[7] M.-F. Lan, A. Tammineedi and R. Geiger. Current Mirror Layout Strategies for Enhancing Matching Performance. *Analog Integrated Circuits and Signal Processing, Kluwer Academic Publishers*, 28:9—26, Jul. 2001.
[8] H. Yaghutiel, A. Sangiovanni-Vincentelli and P. R. Gray. A Methodology for Automated Layout of Switched-Capacitor Filters. In *Proc. ICCAD*, pages 444-447, 1986.
[9] J. D. Bruce, H. W. Li, M. J. Dallabetta and R. J. Baker. Analog Layout using ALAS!. *IEEE J. of Solid-State Circuits*, 31(2):271-274, Feb. 1996.
[10] M. Pelgrom, A. Duimnaijer and A. Welbers. Matching Properties of MOS transistors. *IEEE J. of Solid-State Circuits*, 24(5):1433-1440, Oct. 1989.
[11] R. C. J. Taylor. Switched Capacitor Filters. R. J. van de Plassche *et al*. (eds.). *Analog Circuit Design*: 203-225, Kluwer Academic Publishers, 1995.