Power Crisis in SoC Design: Strategies for Constructing Low-power, High-performance SoC Designs.

K. Brock, Virtual Silicon, US
C. Edwards, Electronic Times, UK
R. Lannoo, Alcatel, BE
U. Schlichtmann, Infineon Technologies, DE
A. Domic, Synopsys, US
J. Benkoski, Nanometer Analysis and Test, US
D. Overhauser, Interconnect Verification, US
M. Kliment, Virtual Silicon, US

Abstract

This special panel session brings together several leading technologists to discuss the challenges and solutions in constructing SoC designs that achieve their performance goals within a very tight power budget. These challenges are addressed from the often conflicting perspectives of semiconductor design teams and commercial solutions providers of EDA construction tools, EDA analysis tools and semiconductor IP (SIP).

Origin of the Crisis

With the addition of high-performance features to battery-operated devices and packages hitting thermal limits in desktop and server devices, automated SoC low-power design methodology is at a crisis. In order for designers to develop algorithms and partition their systems for optimized power, they must depend on a set of power-efficient and accurately power-characterized SIP components (standard cells, memories, I/O, and mixed signal). Designers then construct their SoCs using a long chain of EDA design tools from design planning, simulation, and synthesis, to placement and routing. They must analyze these designs using a chain of extraction and verification tools for timing, power, test, design rule compliance and signal integrity.

Traditionally, synthesis tools have focussed on achieving timing closure, routers with area minimization and floor planners arbitrating between those two often conflicting goals. Dynamic and static power minimization have been relegated to analysis tools that point out problems designed-in by the construction tools. Today's deep submicron CMOS transistors are incredibly dense, amazingly fast, but ravenously hungry in dynamic and static power—often making the task of power optimization the major design challenge. The results are often missed power budgets, larger batteries and heavy heat sinks.

The Controversy

SoC design is a team sport requiring the close coordination of many IC design disciplines with the commercial solutions providers of EDA tools and SoC IP. Specifically:

- What are the most significant power issues?
- Who should drive the SIP power characterization standards shared by the construction and analysis tools?
- Where do designers need the most low power design methodology leadership to be successful and from where is it going to come?