Systematic Design of a 200 MS/s 8-bit Interpolating A/D Converter

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Abstract

The systematic design of a high-speed, high-accuracy Nyquist A/D converter is proposed. The presented design methodology covers the complete flow and is supported by software tools. A generic behavioral model is used to explore the A/D converter's specifications during high-level design and exploration. The inputs are the specifications of the A/D converter and the technology process. The result is a generated layout and the corresponding extracted behavioral model. The approach has been applied to a real-life test case, where a Nyquist-rate 8-bit 200MS/s 4-2 interpolating A/D converter was developed for a WLAN application.

1. Introduction

In the design of analog functional blocks as part of a large system on silicon, a number of phases are identified. These are depicted in Fig. 1. The first phase in the design is the specification phase. During this phase, the analog functional block is analyzed in relation to the surrounding system to determine the system-level architecture and the required block specifications. With the advent of analog hardware description languages (VHDL-AMS, VERILOG-A/MS), the obvious implementation for this phase is a generic analog behavioral model [1]. This model is parameterized with respect to the specifications of the functional blocks. The next phase is the design (synthesis) of the functional block. It consists of sizing & layout and is shown in the center of Fig. 1. The design methodology used, is top-down performance-driven [2,3]. This design methodology has been accepted as the de facto standard for systematically designing analog building blocks [2,4]. Finally, a behavioral model for the block is extracted from the sized circuit including (layout) parasitics. This allows verifying and efficiently simulating the block as part of a larger system. This methodology is now applied to a Nyquist-rate interpolating A/D converter.

The paper is organized as follows. Section 2 explains the chosen A/D converter architecture. In section 3 the systematic design methodology is described in detail and in section 4 the measurement results are given. Finally, conclusions are drawn in section 5.

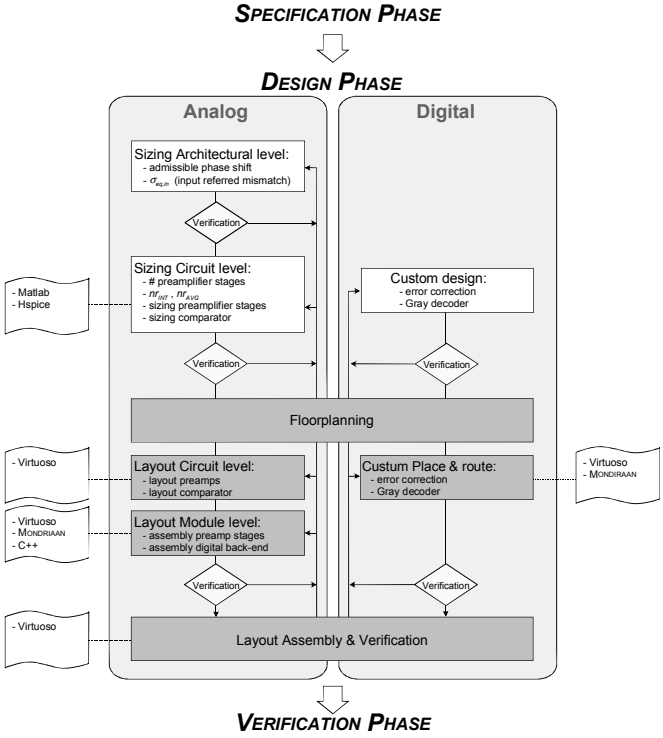

Figure 1: Presented systematic design flow for a Nyquist-rate interpolating A/D converter.

2. The interpolating/averaging architecture

Although a flash architecture offers intrinsically the fastest conversion rates due to its parallel processing, it has the disadvantage of large power consumption and high input capacitance as the number of comparators increases exponentially with the resolution specification. To overcome these shortcomings, analog preprocessing like interpolating, folding and averaging is usually applied [5]. The interpolating/averaging architecture is depicted in Fig. 2. The front-end is fully differential for improved dynamic performance. A Sample & Hold circuit (S/H) samples the differential input signal. The resulting signal is compared and amplified with the fully differential reference ladder network in the first amplification stage. The output of the preamplifier stage is interpolated $nr_{INT,st1}$ times. If needed a second preamplifier stage is added, which is interpolated $nr_{INT,st2}$ times. Both preamplifier stages use averaging to improve static performance [6].

The outputs of the preamplifier stage(s) steer the regenerative comparators. A digital back-end performs additional error correction and encodes the thermometer coder output from the comparators in Gray code, which is synchronized at the output by a latch.

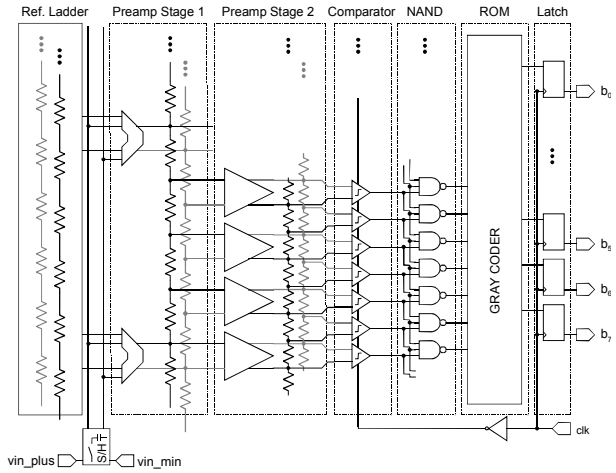

Figure 2: Block diagram of the interpolating/averaging A/D converter architecture.

3. Systematic design of the A/D converter

3.1. Specification phase

The statistical behavioral modeling of A/D converters was covered in [1] and will not be further discussed in this paper. Using this model, the targeted specifications as listed in Table 2 later on, can be explored and determined on system level.

3.2. Design phase

The specifications that are derived during the specification phase are now the input to the design phase. The design of the converter is performed hierarchically. First, some architectural decisions have to be made. Both static and dynamic performance are taken into account, resulting in specifications for mismatch and admissible phase shift for the different building blocks.

Sizing at architectural level

Consider that the offset voltages of all the comparators in a full flash architecture are independent variables with a normal distribution. Then, a Monte-Carlo simulation can be used to estimate the design yield as a function of the total equivalent input-referred offset. For these simulations a targeted INL of 1.0 LSB and a targeted DNL of 0.5 LSB were used. Using averaging techniques, the DNL can be improved by a factor of nr_{AVG}, while the INL can be improved by $\sqrt{nr_{AVG}}$ [6]. This dependency on the amount of averaging nr_{AVG} is implemented in a lookup table for circuit-level optimization. With e.g. an averaging of 9 ($nr_{AVG}=9$) the simulations yield a constraint for the admissible total equivalent input referred offset:

$$\sigma_{total,\,offset} \le 0.7\ LSB \tag{1}$$

From statistical behavioral modeling [1] and technological constraints for the process used (Alcatel Microelectronics 0.35 µm CMOS), it can be calculated that a gain of 15 is sufficient for the comparator to have negligible contribution in the total equivalent input referred offset.

$$\begin{aligned} A_{preamp} &= A_{preamp\_st1} \cdot A_{preamp\_st2} \\ &= f(INL, technology) \ge 15 \end{aligned} \tag{2}$$

In this design A_{preamp} was chosen 20. Thus mismatch and speed no longer have to be traded off for the comparator, allowing to optimize the comparator for speed.

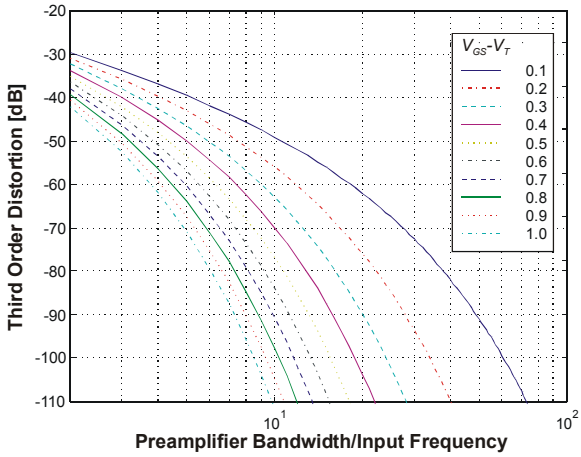

Figure 3: HD_3 as a function of the preamplifier bandwidth/input frequency ratio for a V_{fs} of 1.25 V.

Apart from the mismatch constraint, the admissible phase shift for the preamplifier is also determined in this stage of the design. In [5] a formula was derived for the resulting third-order distortion HD_3 as a function of the bandwidth of the preamplifier stages:

$$HD_3 \approx \frac{2g\ f_{in}}{3\pi\ f_b},\ \text{where}\quad g \approx e^{-2b_n \frac{(V_{GS}-V_T) f_{in}}{V_{fs}\ f_b} - 1} \tag{3}$$

V_{fs} is the full-scale input range, f_{in} is the input frequency and f_b is the bandwidth of the preamplifier, g represents the normalized delay $\delta t_d/BW$ of the preamp, b_n is the relative output level. The normalized delay is worst-case around the mid-codes i.e. when $b_n = 0.5$. The results of equation (3) is depicted in Fig. 3: for this example the targeted 50 dB distortion would result in a constraint of 10° phase shift at Nyquist frequency for a V_{GS}-V_T of 0.3 V:

$$\varphi_{Nyquist} \le \operatorname{atan}\left(\frac{1}{6}\right) \approx 10° \tag{4}$$

Sizing at circuit level

The architectural-level design resulted in constraints in terms of gain ($A_{preamp} > 15$), bandwidth of the preamps

(e.g. $\varphi_{Nyquist} \le \text{atan}\left(\frac{1}{6}\right) \approx 10°$), and admissible input-referred offset (e.g. $\sigma_{total,offset} \le 0.7\ LSB$) for the different building blocks. Using these constraints, each of the building blocks can be sized as will be discussed in detail in the following paragraphs for each block: S/H, fully differential ladder, 1st stage preamplifier, 2nd stage preamplifier, comparator and digital back-end.

The S/H was based on the architecture presented in [7] using the gain-boosting technique. The S/H was designed to steer a load of 5 pF with an input swing of 0.8V. The simulated 3rd harmonic is -68dB and the 5th harmonic is -83dB at a sampling rate of 200MS/s.

The reference ladder has to be properly sized in order to avoid feedthrough. A first-order estimation of the feedthrough to the midpoint of the reference ladder is [8]:

$$V_{mid}/V_{in} = \tfrac{\pi}{4} f_{in} R_{ladder} C \qquad (5)$$

In this formula f_{in} is the input frequency. R is the total resistance in the case of one ladder (typical 100 Ω). C stands for the total coupling capacitance from the input to the reference ladder (the gate-source capacitance of the input transistors of the preamplifiers). With this formula, the maximum resistance of the ladder network is calculated.

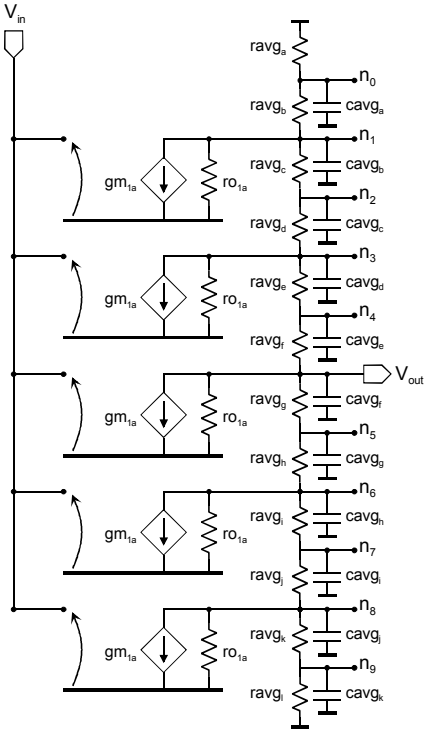

Figure 4: Simplified schematic for preamplifiers in case of nr_{AVG}=5 and nr_{INT}=2.

For the preamplifier the simplified schematic, as depicted in Fig. 4, can be used in combination with the ISAAC tool [9] to calculate a closed expression for the overall gain of the preamplifier:

$$A_{preamp\_st1} = -2 \cdot \frac{gm_{m1}}{g_{AVG}} \cdot \frac{nr_{INT}\left(nr_{AVG}+1\right)^2}{2^3} \qquad (6)$$

This expression is a function of the amount of averaging nr_{AVG} and the number of interpolations nr_{INT}.

The dominant pole is given by:

$$f_{dominant\_st1} = \frac{1}{2\pi \cdot f\left(nr_{AVG}, nr_{INT}\right) \cdot R_{AVG} \cdot C_{load}} \qquad (7)$$

where $f\left(nr_{AVG}, nr_{INT}\right)$ is a fit factor extracted from simulations. This fit factor is a function of both the number of averaging nr_{AVG} and the number of interpolations nr_{INT}. Its value can be found in Table 1.

Fit factor f		nr_{AVG} 3	5	7
nr_{INT}	2	2.30e-2	1.04e-2	5.92e-3
	4	3.53e-3	1.60e-3	9.02e-4

Table 1: Fit factor for dominant pole preamplifier.

The second-stage preamplifier is depicted in Fig. 5. The mismatch contribution is given by:

$$\sigma^2_{in\_st2} = \sigma^2_{m1} + 2\sigma^2_{m3}\left(\frac{gm_{m3}}{gm_{m1}}\right)^2 \qquad (8)$$

A more detailed analysis of this preamplifier can be found in [6]. The power supply of the 2nd stage preamplifier has been separated from the 1st stage preamplifier.

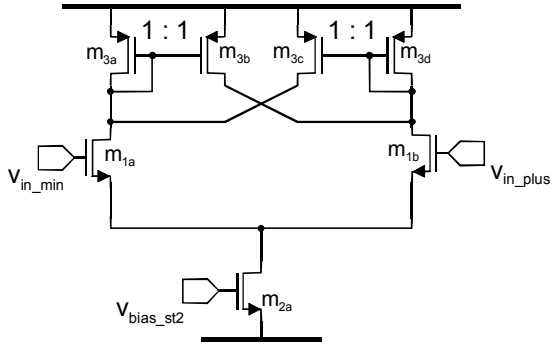

Figure 5: Schematic 2nd stage preamplifier.

The comparator used in this A/D converter is a very fast regenerative structure. A detailed analysis of this regenerative comparator can be found in [10]. After sizing a resulting time constant of 50 ps was simulated.

Combining these equations with the set of constraints resulting from architectural-level synthesis, a full design plan for the converter was derived. The architectural design resulted in three constraints for the design of the preamplifier stages:

$$A_{preamp\_st1} = 10\ ,\ A_{preamp\_st2} = 2 \qquad (9a)$$

$$\varphi_{Nyquist} \le \text{atan}\left(\frac{1}{6}\right) \approx 10° \qquad (9b)$$

$$\sigma^2_{preamp\_st1} \le \frac{3}{4}\left(0.7LSB\right)^2,\ \sigma^2_{preamp\_st2} \le \frac{1}{4}\left(0.7\ LSB\right)^2 \qquad (9c)$$

From these constraints (9), and the complete set of design equations derived, all transistors are sized using advanced simulated annealing [11]. The phase shift constraint is evaluated using equation (3) during optimization. The offset constraint is implemented as a lookup-table and checked as the amount of averaging nr_{AVG} evolves during optimization. The overdrive voltages V_{GS}-V_T of the preamplifiers, the lengths L of the transistors, the biasing currents and the averaging resistor values r_{AVG} are the input variables of the optimization. An overdrive voltage of 0.3 V and 0.2 V was chosen as starting point for the 1st, respectively 2nd stage preamplifier. The input range was fixed during optimization as was the number of interpolations which was chosen $nr_{INT,st1}$=4 and $nr_{INT,st2}$=2. Fig. 6 shows the evolution of the global cost during optimization.

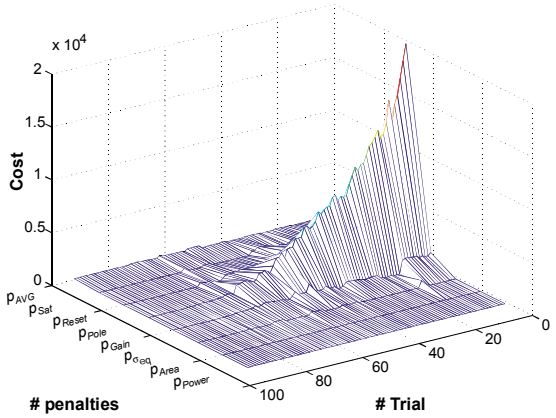

Figure 6: Global cost during sizing using advanced simulated annealing.

Fig. 7 shows the evolution of the cost defined for the pole placement in the different subblocks (1st & 2nd stage preamplifier and comparator).

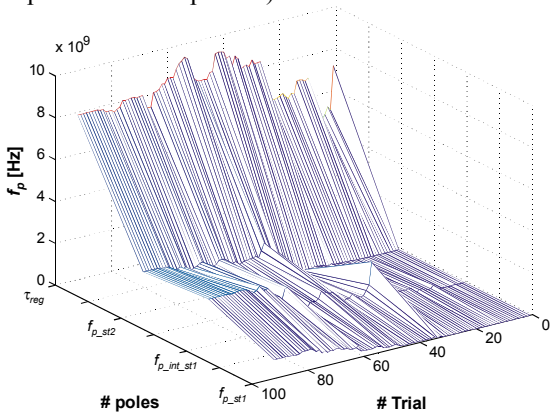

Figure 7: Pole placement during sizing using advanced simulated annealing.

Layout

As the specs push the design closer to the technological boundaries, chip design has become layout driven and parasitics have to be taken into account during design.

The floorplan follows directly from the block diagram in Fig. 2. The result is depicted in Fig. 8: the S/H was inserted on the top. From left to right, the differential ladder network, the 1st and 2nd stage preamplifiers, the comparators and digital back-end are placed.

Analog and digital power supplies have been separated to avoid cross-coupling from the analog to digital part. Around the perimeter of the chip 1 nF of decoupling capacitance has been integrated to provide stable power supplies.

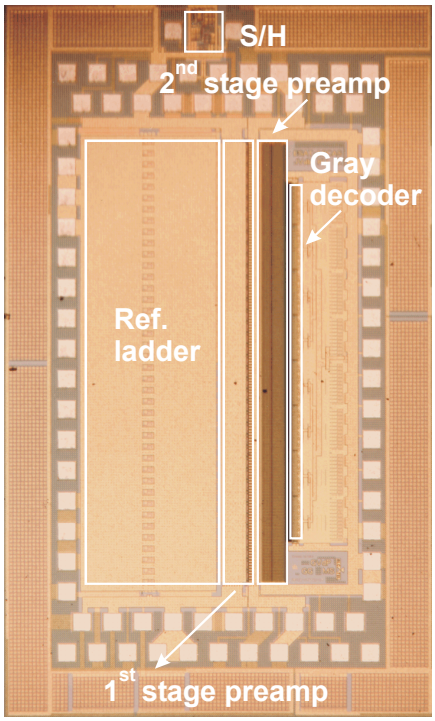

Figure 8: Micro photograph of the A/D converter.

The reference ladder was implemented in metal 1 layer. Dummies were added to provide identical surroundings. An additional decoupling capacitance of 10x30pF was added to each ladder to provide stable reference levels.

The layout of the preamplifiers and the routing was done manually: devices were generated using LAYLA [12], placement of the different modules (1st & 2nd stage preamplifier) was done using MONDRIAAN [13]. Internally, an additional 500 pF of decoupling capacitance was added. Guard rings were used to reduce substrate (digital) noise coupling. A routing channel has been inserted between 1st stage and 2nd stage preamplifiers. Although this kind of task is automated in digital layout, in analog this is still a manual job, as equal delay is important in these connections.

The clock distribution is critical for analog design, and available digital tools cannot deal with the specific analog requirements. A buffered binary clock tree takes care of equal delay, which would otherwise deteriorate the dynamic performance. The design and layout of this clock buffer was done manually.

4. Measurements

The A/D converter was processed in a 0.35µm CMOS process. The A/D converter was mounted on a ceramic substrate and fully characterized. All measurements were done at full speed of 200 MS/s [5]. The S/H was bypassed. The analog preprocessing chain consumes 285 mW, the reference ladder consumes 250 mW and the digital part consumes 120 mW worst case.

The measured static performance resulted in an INL < 0.95 LSB and a DNL < 0.8 LSB.

The dynamic performance is shown in Fig. 10. A Signal-to-Noise-Ratio (SNR) of 44.3 dB is achieved at low frequencies; at 30 MHz a SNR figure of 43 dB was measured. A spectral plot for a 30 MHz input signal is shown in Fig. 9.

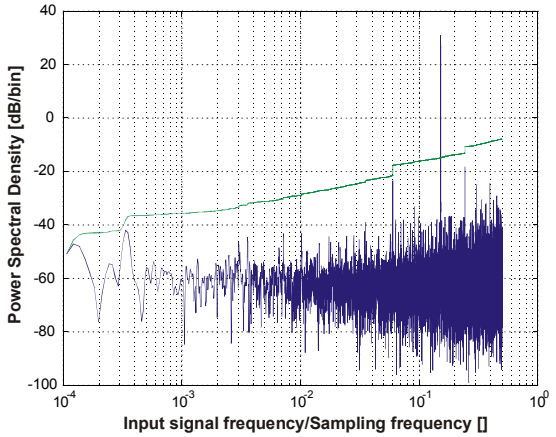

Figure 9: Measured power spectrum for an input signal of 30 MHz.

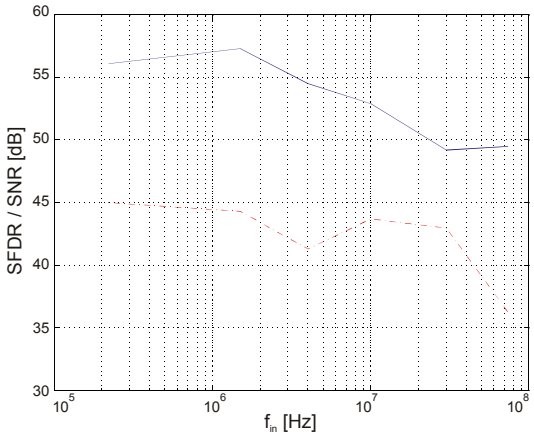

Figure 10: Measured dynamic performance: SFDR>50dB and SNR > 43 dB.

The measured performance is summarized and compared to the specified values in Table 2. All results are comparable to what had been predicted during the sizing.

5. Conclusions

The systematic design of an 8-bit interpolating 200MS/s Nyquist-rate A/D converter has been presented. Using behavioral models the system specifications are translated in offset and phase shift constraints that steer the global optimization at the circuit-level. The chip was processed in a standard 0.35 µm CMOS process. Measurements on the processed chip yielded results that are comparable to the simulated values and predicted high-level specifications. At an input frequency of 30 MHz and at full clock speed a SNR ratio of 43 dB was measured.

Specification	Target value	Simulated	Measured
input capacitance	< 5 pF	4.8 pF	-
input range	> 0.5 V ptp	1.3 V ptp	1.3 V ptp
Latency	not specified	1 clock cycle	1 clock cycle
INL/DNL	< ½ LSB	0.3/0.6 LSB	0.8/0.9 LSB
SFDR	> 45 dB	-	59.2 dB
SNR	> 40 dB	-	44.3dB@1.5MHz 43.7dB@30MHz
Conversion rate	1 code/clock cycle	1 code/clock cycle	1 code/clock cycle
Update rate	200 MS/s	200 MS/s	200 MS/s

Table 2: Measured performance of High-speed A/D converter running at 200 MS/s.

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