A Mixed-Signal Design Reuse Methodology Based on Parametric Behavioural Models with Non-Ideal Effects

Antonio J. Ginés, Eduardo Peralías, Adoración Rueda
Instituto de Microelectrónica de Sevilla (IMSE)
Centro Nacional de Microelectrónica (CNM)
Sevilla, Spain

Natividad Martínez Madrid, Ralf Seepold
Dept. Microelectronic System Design
Forschungszentrum Informatik (FZI)
Karlsruhe, Germany

Abstract

Current System-on-Chip (SoC) designs incorporate an increasing number of mixed-signal components. Design reuse techniques have proved successful for digital design but these rules are difficult to transfer to mixed-signal design. A top-down methodology is missing but the low level of abstraction in designs makes system integration and verification a very difficult, tedious and complex task. This paper presents a contribution to mixed-signal design reuse where a design methodology is proposed based on modular and parametric behavioural components. They support a design process where non-ideal effects can be incorporated in an incremental way, allowing easy architectural selection and accurate simulations. A working example is used through the paper to highlight and validate the applicability of the methodology.

1. Introduction

The huge increase in integration capability makes possible to design Systems-on-Chip (SoC). Typically, these SoCs are programmable general-purpose systems integrating at least one processor core and memory. They also need to integrate real-world interfaces, like audio and video range data converters or phase-locked loops.

The design of such complex mixed-signal systems requires a drastic change of methodology. In the last years, the design of digital systems has been accelerated by applying platform-based design reuse of Intellectual Property (IP) modules [3]. The idea behind design reuse is to create IPs for SoC that can be applied in future developments. The main requirements for these components are reduced costs and a wide feature-set, which allow their reusability in a broader family of products

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Analogue and mixed-signal (AMS) IPs are needed both in traditional analogue designs and in mixed-signal SoCs. There are already some standardization initiatives and research approaches to AMS IP, and some companies are offering AMS cores. The AMS Development Working Group of the Virtual Socket Interface Alliance (VSIA), a standardization organization for the design and exchange of IP, has already delivered its second specification document [14].

However, analogue and mixed-signal IPs are much more difficult to achieve than digital IPs. One of the main reasons is that analogue design automation is far beyond the digital one, due to the inherent complexity of analogue systems. In general, behavioural analogue synthesis is in a very early research stage and the entry point to analogue design is the level of transistor netlists.

To allow top-down design and bottom-up verification, it would be desirable to have also behavioural descriptions of the AMS cores. This high-level description would help in the selection of the core, and to speed-up the co-simulation with the digital part. It should be possible to reflect the real characteristics of the core in an accurate manner.

The aim of this work is to define a design reuse methodology for mixed-signal systems, which would incorporate in its portfolio behavioural libraries of AMS cores. In a larger case study, the methodology is being used to build a library of components for telecommunication applications. As an example, the model for a pipeline ADC will be presented.

2. State of the art

Some research groups are working in the area of behavioural libraries for analogue and mixed-signal reuse. Two of them, the FhG Dresden IIS/EAS [5] and the Nokia Research Center [16] have reported on new results developing an environment in the frame of a library of parameterised analogue and mixed-signal blocks with numerical and behavioural models.

Traditionally, analogue and mixed signal blocks modelling, as data converters, has been realised at device level or at a low functional level ([8], [13], [15]). This allows accuracy and good modelling of the non-ideal effects presented in the data converter (noise, distortion, mismatching, etc) but the simulation time increase drastically and technology and architecture independence can be lost. However, with the increasing complexity of designs, the need for accurate and speedy models has produced a change to the current trend towards high functional level designs ([2], [9], [10], [11]). The main advantage of the behavioural level description is the reduction in the simulation speed and the process independence. In Table 1, the two different approaches are compared.

Table 1: Device model vs. Block model

Non-ideal effects	Device model	Block model
Static non linearities	Very high accuracy	High accuracy
Dynamic aspects	Very high accuracy	High accuracy
Noise and matching	High accuracy	Mid accuracy
Speed	Low	High
Reusability	Low	High

3. Design flow

The proposed platform-based mixed-signal design reuse methodology is depicted in Figure 1. Following a top-down design, the requirements for the new system will guide the platform selection. Each platform has a particular portfolio associated, including AMS IPs, also called Virtual Components (VC). Before incorporating the cores into the portfolio, a quality check will prove compliance to standards (VSIA) and to coding guidelines. Each of the

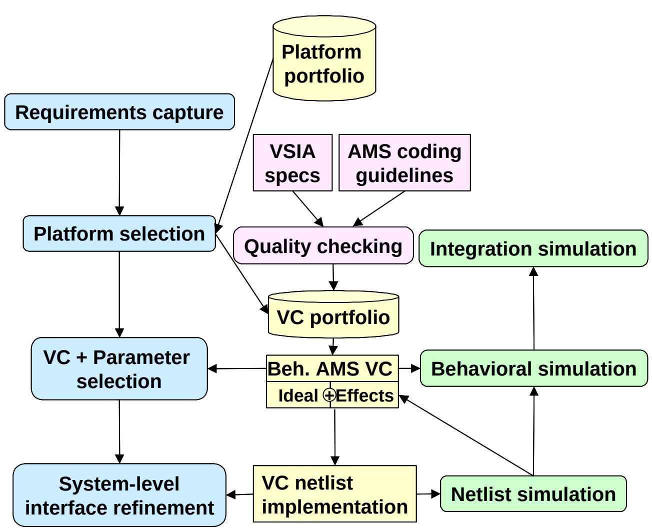

Figure 1: Mixed-signal reuse design flow

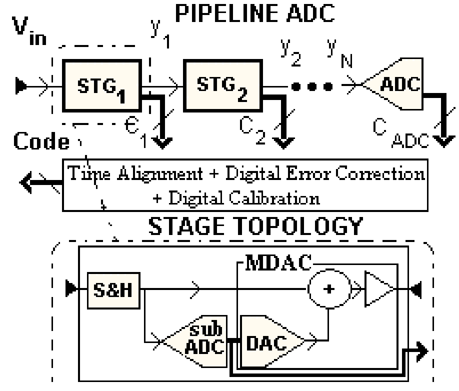

Figure 2: Basic architecture of a pipeline ADC

components will also have a behavioural description, in order to allow a fast selection of cores and parameters. These high-level models will describe different non-ideal effects in a modular way. The parameters of these effects will be incrementally adjusted, and therefore, reflect the real values of low-level descriptions of the block. This will permit a fast but realistic bottom-up simulation of the whole system.

The present methodology is based on the high level of reusability in the AMS IPs, achieved through modularity and parameterisation.

4. Case study

The reusability aspects are going to be analysed by presenting the study of a Pipeline ADC with digital correction and self-calibration, centring the discussion in the analogue part. This model has been realised using a complete VHDL-AMS description.

An accurate Pipeline ADC model needs to describe not only the ideal behaviour, but also the non-ideal effects presented by this kind of data converter. However, non-ideal effects are highly dependent on the architecture and wished performance. Therefore, for an accurate modelling, the non-ideal modular effects have to be included at the block level.

Modularity. The main blocks in the analogue part of a Pipeline ADC are the Sample&Hold, the sub-ADC and the MDAC (Fig. 2). These devices have been selected at the starting point in the analogue part description. In order to increase the modularity of the model, the different non-

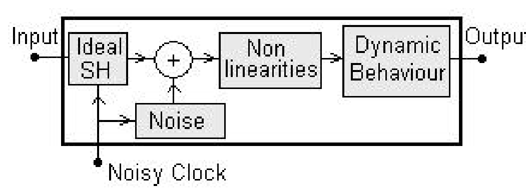

Figure 3: Sample&Hold block

ideal effects have been integrated in separate modules: noise, clock jitter, non-linearities and dynamic behaviour. The complete block model can be obtained interconnecting the planned non-ideal modules to the ideal one. For the Sample&Hold block, this is illustrated in Figure 3. General aspects in the modular implementation are:

Static Behaviour

- Ideal: It defines the ideal behaviour of the block.
- Noise: It introduces a noise component in the input signal.
- Clock Jitter: The developed model only takes into account the uncertainty in the clock signal itself. The internal clock jitter has nor been modelled.
- Non-linearities: This module introduces the non-linearities, the gain and offset in the global block. The non-linearities descriptions is strongly dependent on the particular block. Thus, an independent module has been developed for each device: S&H, sub-ADC and MDAC. For example, an analytical model can be selected:

$$Output = In + a \cdot \left(1 - In^2\right)^m$$

Where: $In = gain \cdot Input + offset$

gain, offset: associated gain and offset

α, *m*: model constants

Dynamic Behaviour

- Filtering: It limits the spectral input signal contents. It is described in the *s* domain.
- Slewing: It limits the output slope. This module has only been considered in the MDAC block.

Parameterisation. All the blocks have been parameterised for an easy integration and reuse of the components in others blocks or designs.

In the current Pipeline ADC model, all basic blocks (S&H, sub-ADC and MDAC) share the noise and filter modules, but with different parameters.

5. Results

This section analyses the technical aspects related to the developed Pipeline ADC such as VHDL-AMS model and simulation results. A Pipeline ADC architecture (Fig. 4) is a good compromise between resolution and velocity. These characteristics are needed in many telecommunications designs where the level of resolution and high speed are rapidly increasing.

5.1. VHDL-AMS model

Nowadays, there are some tools available that support a VHDL-AMS description such as: ADVance MS [7], VeriasHDL [1], TAURITM [6], SMASH [4] and Hamster [12]. Thus, modelling with VHDL-AMS is becoming a serious alternative to the traditional analogue description in Spice.

The complete Pipeline ADC model has been described in VHDL-AMS (analogue and digital part), using ADVance MS v.1.2_2.1 for the compilations and simulations.

The aimed specification is a general model in which the number of the different stages is parameterised producing automatic hardware reconfiguration. VHDL-AMS is a very extensive and powerful language. It includes several constructs that allow to model with a high degree of parameterisation: electrical and multi-dimensional arrays, and supports the generate command. However, due to the complexity of the standard, it is very difficult for a tool to cover it completely. The latest version of the used tool has already enlarged its VHDL-AMS subset. Therefore, it is expected that in the near future, all the parameterisation and reconfiguration could be done inside the tool. Currently, parameter-dependent code generation is implemented using scripts, for instance to generate the different stages.

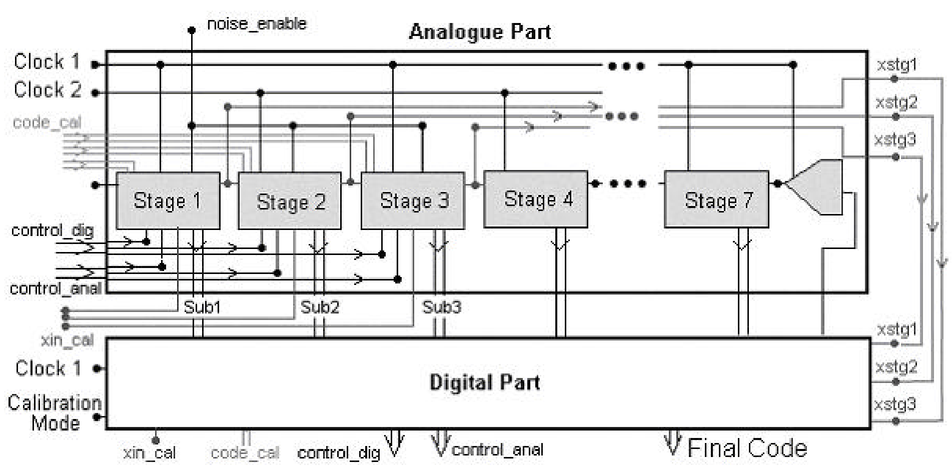

Figure 4: Schematic of the VHDL-AMS Pipeline ADC implementation

For the case study, a Pipeline ADC with a total resolution of 15 bits has been implemented. Its main characteristics are:

- Digital correction: Unit redundancy
- Sel-calibratation: Three first stages calibrated.
- Configuration: 3 3 3 3 3 3 3 1
- Operations controlled by two different clocks

5.2. Simulations

To validate the global model proposed, several simulations have been performed. The modularity conception that dominates the complete system is going to be highlighted in an easy example (Sample & Hold, Fig. 3). It can be noticed (Fig. 5) how each sub-module introduces a perturbed component in the value captured by the Sample & Hold. According to this figure the analogue input is sampled ideally. This process is controlled by a clock that includes a noise component (clock jitter). After the signal is sampled, a noise level is added in order to describe the different noise processes inside the circuits, such as thermal noise, aperture period, etc. Finally, the non-linearities and the dynamic behaviour are included.

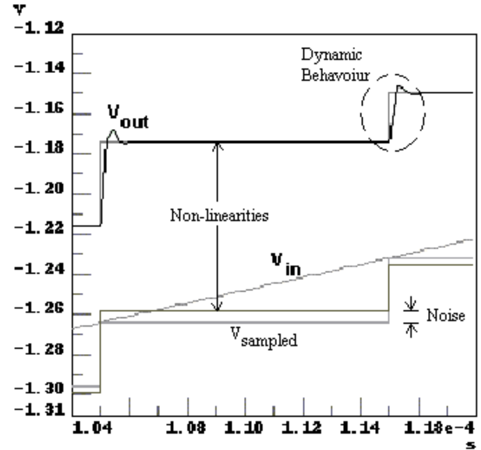

Figure 5: Sample&Hold Simulation

The complete Pipeline ADC simulation has been realised for a sampling frequency of 80 Ms/s and a voltage reference of 2 $V_{pp.}$ The parameters that model non-ideal effects have been selected independently for each stage and block. In Figure 6, the inl and the dnl for the Pipeline

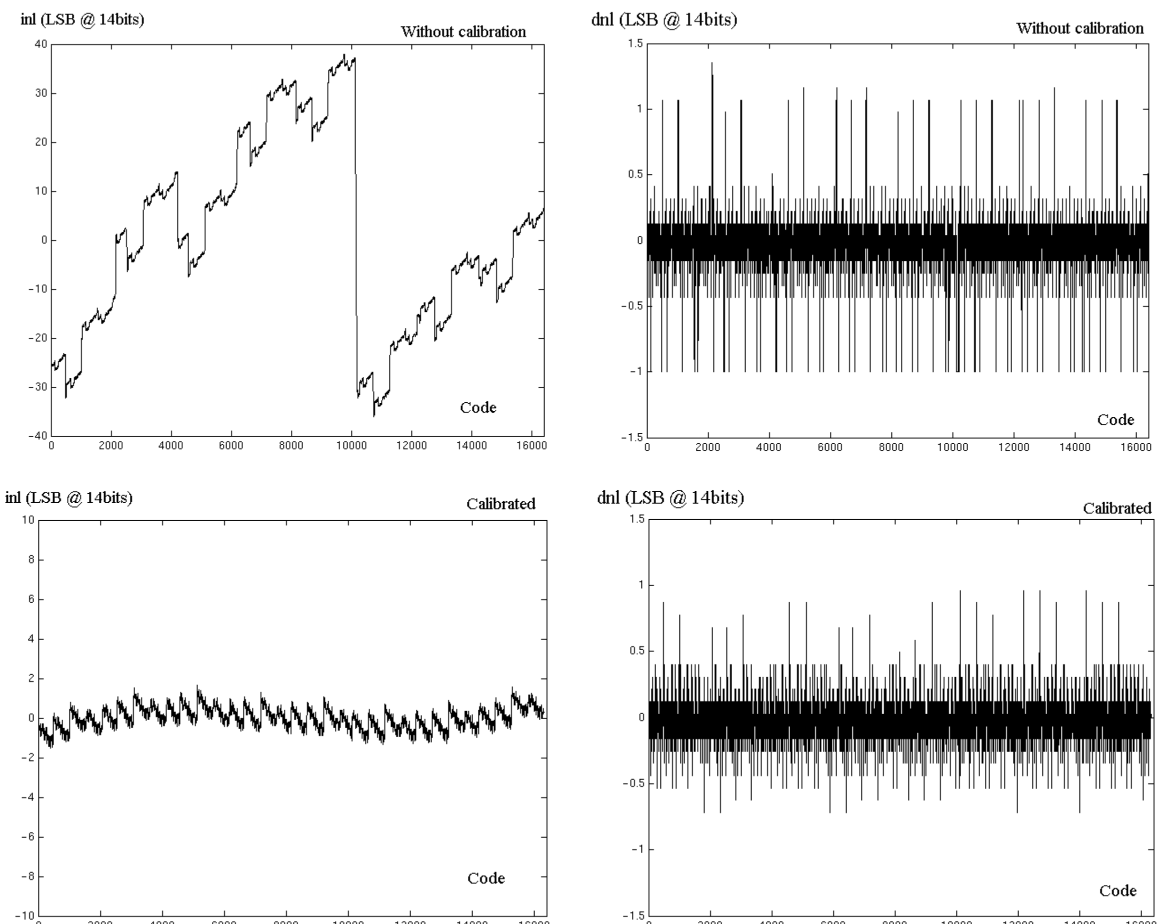

Figure 6: Non-linearities characteristics

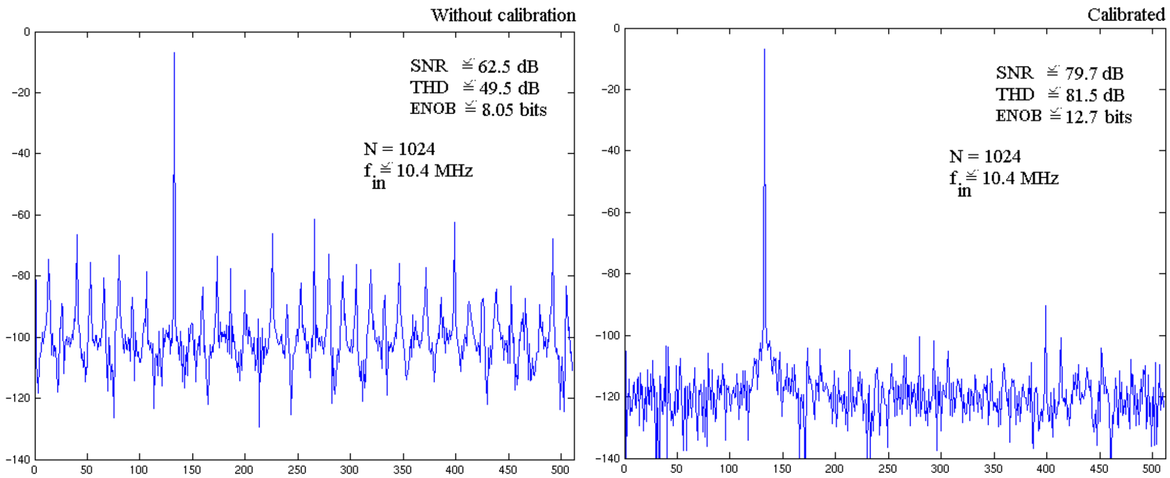

Figure 7: Spectral analysis

ADC without and with calibration are shown. When the calibration is performed, the improving in the linearities specifications is evident. This simulation has been obtained taking into account a ramp input signal. Figure 7 plots the spectral contents for the calibrated and non-calibrated output in the case of a sinusoidal input (fin = 10.39 MHz, 1.8 V_{pp}).

The above simulations show how the high level model takes into account the non-ideal effects (noise, non-linearities, distortion, etc.) necessary for fast core selections in the AMS reuse methodology.

6. Conclusion

This paper has presented a mixed-signal reuse methodology based on abstract behavioural models. The modularity and the high degree of parameterisation of the models increase their reusability.

By using VHDL-AMS, a standard hardware description language, the models can be easily exchanged and have a good tool support. The simulation is very fast and produces very accurate results, thanks to the inclusion of non-ideal effects in models.

Further work is being developed in a class-based attribute and parameter set definition for the mixed-signal models, and in enlarging the telecommunications data converters library.

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