EDA Tools for RF: Myth or Reality?

Organizers:
Luciana Guarnieri – Barcelona Design, Inc.
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Moderator:
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Presenters:
Section I:
Simulation challenges facing the RFIC industry
Dr. Scott Savage, Modeling Group Leader
Cypress Semiconductors

Section II:
EDA tools for RF: myth or reality?
Dr. Mar Hershenson, Chief Technology Office
Barcelona Design, Inc.

Section III:
RF CMOS Design—Big issues, Big rewards
Dr. Xisheng Zhang, VP of R&D, Device Modeling
Celestry Design Technologies, Inc.

Format:
This hot topic session will consist of three talks (about 20 minutes each) from Cypress Semiconductors, Celestry Design Technologies and Barcelona Design, Inc.

Abstracts:

Section I
Simulation Challenges Facing the RFIC Industry

Designing circuits that operate at radio frequencies (above 1 GHz) is a challenge for many reasons. Nearly every aspect of producing chips is stressed at high frequency, including technology development, modeling, CAD, design, integration, and packaging. From a device modeling perspective, devices have shrink to extreme dimensions to achieve the required high frequency performance metrics, while exotic materials are being added to the process. This is straining the limits of industry standard models, as newer, more capable device models struggle to reach the level of generic support necessary to achieve widespread adoption. Substrate currents and losses, device and substrate noise, and device mismatch all need to be accurately modeled as well in RF design.

Electromagnetic effects (both desirable and parasitic) are also much more significant as operating frequencies rise. Lumped RC networks

are no longer sufficient to represent interconnect parasitics. Inductive coupling is now significant on chip, while packages and boards are larger today (relative to the wavelength of operation) than ever before, requiring fullwave electromagnetic simulation. Integrated passives (on chips and packages) have significantly reduced integration costs, but require accurate high frequency models that can be incorporated into analog simulators.

Finally, hierarchical, block based, mixed signal design methodologies are very complicated and not currently well integrated into EDA tools. The models for interaction between blocks is often too simplistic and the coupling between analog and digital components on a chip is often ignored. The result can be resignation to designing in silicon, which keeps design cycle time and the cost of advanced RF chips high.

This presentation will present details of the issues mentioned above to help the audience understand the complexity and depth of the problems, and serve as an invitation to the EDA industry to present solutions to the issues.

Section II
RF Design:
Innovative Approaches, Effective Design

The increased demand for communications and wireless systems combined with the desire to reduce costs by offering integrated system-on chip solutions has generated tremendous interest in the use of RF CMOS circuits. However, the lack of accurate and easy to use models, the complexities associated with high frequency transmission line effects and the undesirable noise interactions between analog and digital blocks severely limit the development of single chip solutions. Unfortunately, conventional simulators (such as Spice/Spectre) take unacceptably long times to run complex RF circuits and suffer from the fact that they are more verification tools rather than design tools. Therefore, a significant paradigm shift is necessary to create practical, efficient and successful EDA tools for RF.

The key to innovating a fast and automated approach to RF design lies in a willingness to employ more accurate nonlinear models within an efficient class of mathematical problems such as convex optimization. In addition to being much faster and accurate than the conventional approach, this methodology also allows the expertise and experience of RF circuit designers to be captured prior to the design execution. Because the capture of

RF knowledge only needs to be done once for each topology, the design process can be greatly sped up allowing process migration and specification changes to be incorporated easily. Since layout information (including floor plan, parasitic effects and matching constraints) can also be incorporated prior to the optimization, a complete RF design flow from specifications to GDSII becomes viable.

Section III:
RF CMOS Design —
Big Issues, Big Rewards

RF CMOS is playing an ever-increasing role in the design of a wide range of devices. Most recently, it has garnered much attention as a viable option for helping enable communication devices, bluetooth, 802.11 and other wireless applications. While many have jumped on the RF CMOS bandwagon, others are quick to point out its limitations.

This presentation will debate the pros and cons of RF CMOS design and related modeling. Will, for example, access to tools for accurate RF simulation convince the nay sayers of the viability of RF CMOS design? And, if so, what will it take to achieve this accuracy?

This debate will present technologists from both camps as they battle over the big issues and big rewards of RF CMOS design using real-life design examples and applications. Included will be discussion of needed and potential breakthrough technologies to aid RF CMOS to become more viable.