Dual Threshold Voltage Domino Logic Synthesis for High Performance with Noise and Power Constraint

Seong-Ook Jung*, Ki-Wook Kim† and Sung-Mo (Steve) Kang‡

* Department of Electrical and Computer Engineering, Univ. of Illinois at Urbana-Champaign, USA.
† Pluris, Inc., 10455 Bandley Dr., Cupertino, CA 95014, USA.
‡ Baskin School of Engineering, Univ. of California at Santa Cruz, USA.

Abstract

We introduce a new dual threshold voltage technique for domino logic. Since domino logic is much more sensitive to noise, noise margins have to be taken into account when applying dual threshold voltages to domino logic. To guarantee the signal integrity in domino logic, we carefully consider the effect of transistor sizing and threshold voltage selection. For optimal design, tradeoffs need to be made among noise margin, power, and performance. Based on the characteristics of each logic gate, we propose noise and power constrained domino logic synthesis for high performance. ISCAS85 benchmark results show that performance can be improved up to 18.62% *with* 2% *active power increase, while maintaining noise margin.*

1 Introduction

A common technique in high-performance chip design is to exploit dynamic logic such as domino CMOS circuits in critical portion of the chip [5]. The drawbacks of domino logic are high noise sensitivity due to dynamic node, and incomplete logic family excludes inverting logic such as NAND function [3]. Nevertheless, chip designers need to use domino logic in performance critical path. Low power consumption has been one of the major issues in VLSI design. Supply voltage scaling is an effective technique to reduce power consumption although it can slow down the speed. To compensate for performance degradation due to supply voltage scaling, threshold voltage (V_t) needs to be scaled down accordingly. However, (V_t) scaling accompanies the exponential increase in subthreshold current (I_{sub}) of transistors.

To tackle the high leakage current problem, dual V_t techniques [6, 7] have been proposed for static CMOS logic. They use high V_t devices off critical paths to reduce the leakage current, while using low V_t for transistors on critical paths to maintain high performance. Such approaches mainly focus on the minimization of leakage power. Since static CMOS logic is less susceptible to noise than domino logic, it is assumed that the variation of noise margin due to threshold substitution is negligible.

In domino logic, I_{sub} is a concern for not only static power consumption but also noise margin. In [4], a technique is proposed to make all domino logic gates evaluated in standby mode to save the leakage current without considering noise immunity. Not much research has been done on the noise margin variation caused by low V_t assignment. The authors in [8] analyze the noise sensitivity of domino logic and recommend to use low V_t only in static logic. To resolve the trade-off between performance and noise margin, a keeper control method in clock delayed domino logic has been proposed in [1, 2]. In practice, it is difficult to synchronize the clock delay and the signal delay such that the data arrival is matched with the evaluation clock edge.

In this paper, we characterize the effect of keeper sizing and dual V_t on noise margin, performance and power consumption. Associated with noise characterization, the tradeoff is analyzed among the speed, active power consumption in active mode, and the leakage current in standby mode. Finally, we propose dual V_t domino logic synthesis method. It uses low V_t devices according to logic gate types to speedup evaluation while minimizing power consumption and maintaining noise margins.

2 Noise and Keeper Sizng in Domino Logic

2.1 Noise Constraint

Domino logic is intrinsically more sensitive to noise than static logic. In UDSM technology, cross coupling noise gets even worse since interconnection layers are packed closer together and the interconnections are made thicker to reduce its sheet resistance. Furthermore, V_t scaling exponentially increases I_{sub}. As a result, the dynamic node becomes more vulnerable due to potential crosstalk combined with discharge by subthreshold leakage current.

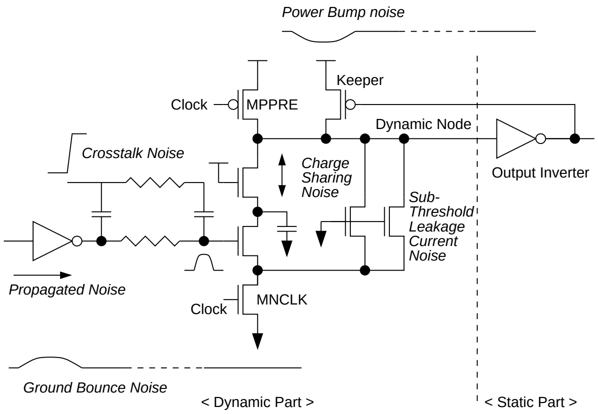

Figure 1. Noise sources of domino logic

Figure 1 shows noise sources of domino logic such as crosstalk, subthreshold leakage current, charge sharing, power supply bump and ground bounce.

We apply the static noise constraint defined in [1, 8] to each domino logic gate to determine the keeper transistor size.

$<$ Noise Constraint $>$

Suppose the input to the topmost NMOS transistors that are directly connected to the dynamic node is 20% of power supply (V_{dd}), and the other NMOS transistors turn on with V_{dd}. Then, the domino logic is considered to fail if the output voltage of inverter is greater than 10% of V_{dd}.

2.2 Noise Margin

In domino logic design, high-skew output inverter with high P:N ratio, namely, (PMOS transistor width)/(NMOS transistor width), is commonly used to accelerate evaluation by reducing logic trip point. However, as the P:N ratio increases, the output inverter is more likely to switch erroneously with small noise pulse. Thus, a slight voltage variation in the dynamic node can trigger logic transition. If low V_t is applied to the PMOS transistor of output inverter in order to make the evaluation faster, then low V_t PMOS transistor further aggravates the noise margin.

When low V_t is applied to NMOS transistors in the evaluation tree, the evaluation of NMOS tree becomes faster. In this case, significant subthreshold leakage current can flow from dynamic node to ground through low V_t NMOS tree. Such considerable leakage current lowers the noise immunity of domino logic. The worst case corresponds to a multi-fanin OR gate with extremely low trip point.

2.3 Keeper Sizing

There are tradeoffs between evaluation time and noise margin. To improve the evaluation time for a given circuit implemented with high V_t transistors, low V_t can be applied to the NMOS transistors in the evaluation tree and/or the PMOS transistor of high-skew output inverter. In those cases, evaluation time is improved but noise margin is degraded as discussed in Section 2.2. Unless we resize the keeper appropriately, the domino logic may fail since it can not meet the noise constraint due to reduced noise margin. Therefore, keeper sizing is essential in dual V_t domino logic design accounting for performance, power and noise.

The bigger the keeper transistor is, the more contention takes place between the keeper and the NMOS transistors in the evaluation tree during evaluation. As a result, the short circuit current increases, which increases power consumption in active mode. In terms of evaluation time, increased keeper size can reduce the benefits of the low V_t replacement and the high-skewed inverter. Worse yet, if the keeper size is made too big to overcome significant I_{sub} through low V_t transistors, the evaluation time of domino logic can be longer than that of domino logic with high V_t NMOS transistors in the evaluation tree [1].

To sum up, noise margin depends on the P:N ratio of output inverter and threshold voltage assignments. The keeper transistor has to be properly sized to minimize power consumption within noise constraint. The effect of keeper sizing on evaluation time, total power consumption in active mode, and leakage current in standby mode varies according to logic gate types. Simulation results for different logic gate types are shown in the next Section.

3 Simulation Results and Comparison

All HSPICE simulations have been performed using model parameter based on 0.13 μm CMOS process and operating voltage of 1.2 V. Table 1 shows the delay time and I_{sub} characteristics with values normalized with respect to high V_t transistor, for low and high V_t transistors.

Table 1. Performance and subthreshold leakage current of low and high V_t transistors

Transistor Type	Delay Time	Sub-Threshold Leakage Current
High V_t	1.0	1.0
Low V_t	0.78	3.9

The precharge PMOS transistor and the NMOS transistor of output inverter are fixed to high V_t since the precharge time is less important than evaluation time. Those transistors determine the leakage current in standby mode if we assert all domino logic gates to be evaluated in the standby mode [4]. We consider four cases of the low V_t assignment to NMOS tree and/or PMOS transistor of output inverter. As shown in Figure 2, there are four combinations of feasible configuration according to V_t assignment, namely HH, HL, LH, and LL types. The first character H (or L) denotes high (or low) V_t NMOS tree, and the second character H (or L) denotes high (or low) V_t PMOS transistor of output inverter.

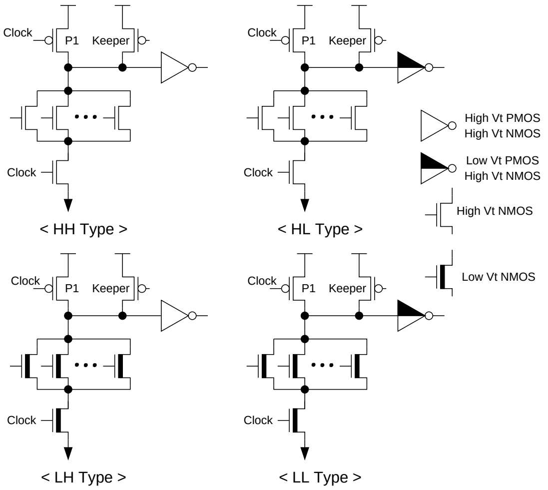

Figure 2. Feasible configuration with low V_t transistors

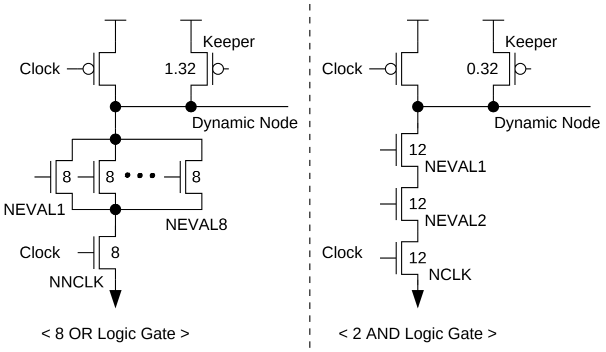

Figure 3. Keeper size of case 1 (HH type)

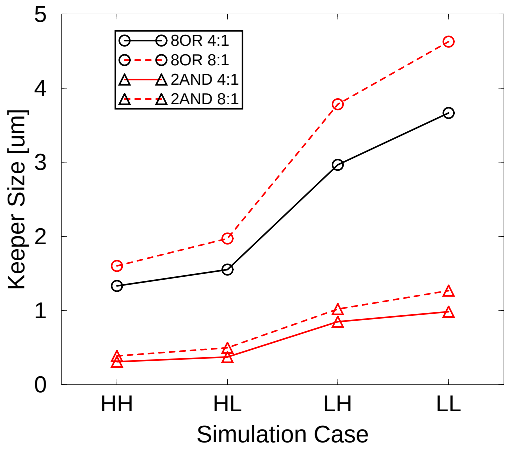

Figure 4. Keeper size based on transistor size of Figure 3

3.1 Keeper Sizing for Feasible Configurations

Figure 3 shows the example of keeper size for 8-input OR and 2-input AND gates of HH type with 4:1 P:N ratio output inverter, where keeper size denotes the width of keeper transistor and lengths of all transistors are set to the minimum channel length. Keeper sizes are properly chosen to guarantee the noise constraint specified in Section 2.1. Keeper size depends on V_t combinations and logic gate types and P:N ratio of output inverter as shown in Figure 4. As the P:N ratio of output inverter increases, the noise margin of output inverter decreases. Thus, the keeper of logic gate with 8:1 P:N ratio output inverter is bigger than that of logic gate with 4:1 P:N ratio output driver for all simulation cases.

For 8-input OR gate, the keeper size is determined by I_{sub} of all 8 NMOS transistors in the evaluation tree, since all the transistors account for the subthreshold current flowing from dynamic node to ground. However, for 2-input AND gate, its keeper size is determined only by the topmost NMOS transistor in the evaluation tree. Other NMOS transistors in the evaluation tree are assumed to be on for noise margin consideration as mentioned in Section 2.1. Therefore, the keeper transistor for 8-input OR gate is much wider than that of 2-input AND gate for all V_t combinations.

When applying low V_t to NMOS transistors in the evaluation tree and/or PMOS transistor of the output inverter, the keeper should be up-sized to ensure noise immunity as mentioned in Section 2.3. It should be noted that the keeper for LH type is far wider than that for HL type as shown in Figure 4. The reason is that significant amount of I_{sub} flows via evaluation tree since low V_t NMOS transistors in the evaluation tree constitute a direct current path from dynamic node to ground. Therefore, the keeper transistor needs to be wide enough to compensate for the charge leakage due to I_{sub}. Meanwhile, there is a low V_t subthreshold leakage current path between power supply to output node of output inverter for HL type configuration. The amount of I_{sub} can be reduced exponentially by increasing the gate voltage of the output inverter. Therefore, smaller keeper is sufficient to meet the noise constraint for HL type compared to LH type configuration.

3.2 Evaluation Time, Power in Active Mode and Leakage Current in Standby Mode

Evaluation time (t_E) and total power consumption (P_{act}) in active mode are measured at 500MHz operating frequency. The leakage current (I_{leak}) is measured in standby mode by making all logic gates evaluated to reduce leakage current.

Figure 5, 6 and 7 show the simulation results for 8-input OR gate and 2-input AND gate.

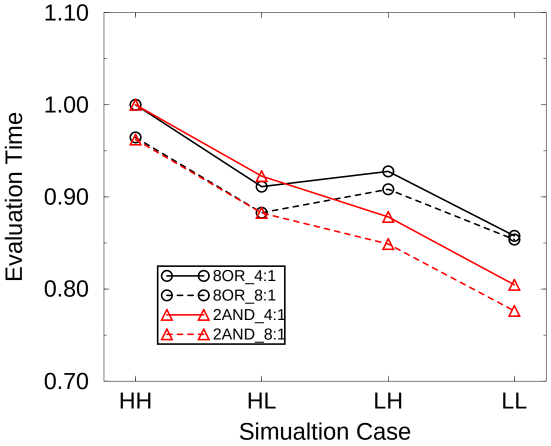

Figure 5. Evaluation time (t_E)

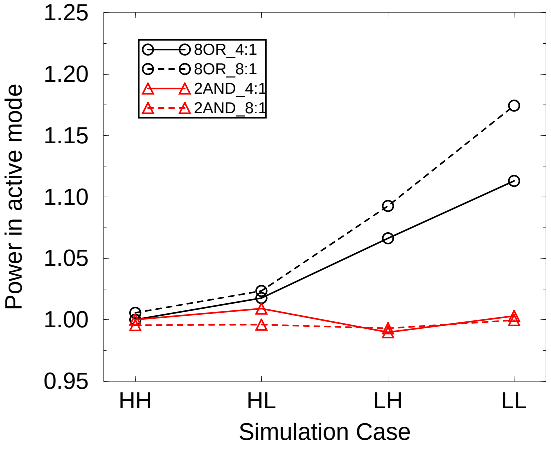

Figure 6. Power consumption in active mode (P_{act})

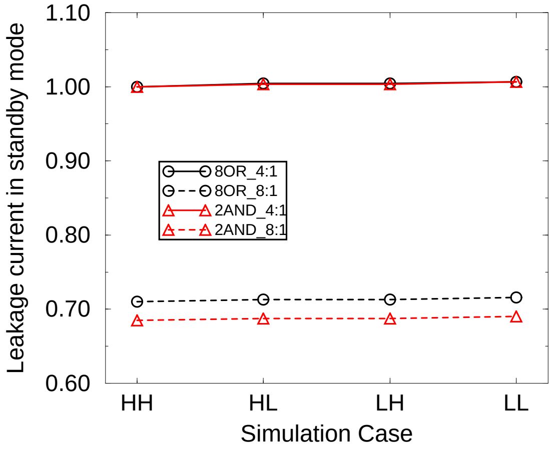

Figure 7. Leakage current in standby mode (I_{leak})

The values of t_E, P_{act} and I_{leak} are normalized by HH type of each gate with 4:1 P:N ratio output inverter. First, we analyze the simulation result of domino logic gate with 4:1 P:N ratio output inverter. Then, we analyze the effect of up-sizing PMOS transistor from 4:1 to 8:1. For both 8-input OR and 2-input AND gates, LL type has the fastest speed while consuming the highest total power in active mode.

In case of 8-input OR gate, LH type is slower than HL type since the benefit of low V_t NMOS transistors in the evaluation tree for t_E is lessened by much bigger keeper size as shown in Figure 4. The P_{act} of LH type is greater than that of HL type since the short circuit current increases through the conduction path of wider keeper transistor and NMOS transistors in the evaluation tree. I_{leak} is determined by precharge transistor (MPPRE) and NMOS transistor of output inverter since all domino logic gates assumed to be evaluated in standby mode. MPPRE and NMOS transistor of output inverter have the same size and V_t. Thus, I_{sub} is almost the same for all the simulation cases. Therefore, for 8-input OR gate, HL type shows better performance and power characteristic than LH type.

For 2-input AND gate, LH type is faster than HL type for the following reasons. For evaluation time, the effect of stacked NMOS transistors in the evaluation tree is greater than that of PMOS transistor of output inverter. And the keeper size of LH type is small compared to NMOS transistor size in the evaluation tree even though it is bigger than that of HL type. P_{act} in active mode is almost the same for all V_t types in 2-input AND gate. The reason is that the increased power by the contention between keeper and NMOS transistors in the evaluation tree for LH type is compensated by the decreased short circuit power in output inverter according to steep switching slope of dynamic node. And the keeper size of HL type is comparable to the keeper size of HH type.

Now we analyze the effect of P:N ratio of output inverter. t_E is improved by increasing the P:N ratio. But for LL type of 8-input OR gate, t_E values for 4:1 and 8:1 P:N ratio are almost the same since bigger keeper size lessens the high-skewed effect. P_{act} is almost the same for all 2-input AND gate in all simulation cases. But for 8-input OR gate, P_{act} increases as the P:N ratio of output inverter increases. I_{sub} is almost decreased by 30% by changing P:N ratio from 4:1 to 8:1. But, extremely high-skew output inverter is much more susceptible to coupling noise because of small size of NMOS transistor of output inverter. The amplitude of coupling noise on the output of the inverter cannot be easily decreased over time since small NMOS has weak driving capability. In effect, the next stage domino logic gates will see stronger input noise.

4 Low V_t Selection for High Performance with Noise and Power Constraint

The dual V_t assign problem can be viewed in two perspectives: either to optimize delay under power constraint or to minimize the power under delay constraint. In this work, we propose a method to minimize delay under noise and power constraints. We assume that a given circuit has all high V_t transistors initially. Figure 8 shows the proposed dual V_t domino logic synthesis flow.

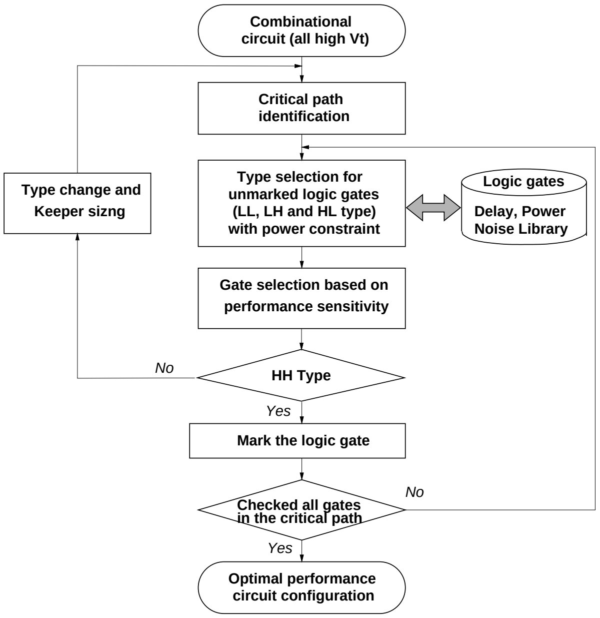

Figure 8. Dual V_t domino logic design flow

At first, the critical paths of a given circuit are identified based on static timing analysis. For each gate in the critical paths, a proper type is selected for delay minimization with power constraint. Here, it should be noted that the V_t combinations (HH, LL, LH or HL type) determine the behavior of the domino logic as shown in Figure 5, 6 and 7. For instance, in 8-input OR gate, the LL type shows the fastest switching time with maximum power. If LL type satisfies the power constraint of the whole circuit, then the OR gate is tagged with LL type which will be used in performance sensitivity computation. Otherwise, HL type is tested next. It is unnecessary to test for LH type, since LH type is not only slower than HL type, but also consumes more power than HL type.

The order of type selection depends on logic gate types. For instance, 8-input OR gates are checked in the order of LL type and HL type. Meanwhile, 2-input AND gates have a different priority of type selection such as LL type, LH type and HL type. The key point here is that trade-offs among performance, power and noise sensitivity are precharacterized for *each logic gate type*. Dual V_t domino logic design has to be driven by the features depending on the incorporated logic function.

After selecting feasible types for all gates in the critical paths, a gate is chosen such that performance of the gate is maximum. Performance sensitivity is defined as

$$\text{performance sensitivity} = \frac{\Delta t_E}{\Delta P_{act}}. \tag{1}$$

Then, low V_t is applied to the gate according to the selected type and the keeper transistor is sized to meet noise constraint.

Threshold substitution can modify critical paths in a circuit. Thus, we need to identify new critical paths after the modification. Low V_t application is iteratively carried out until no more speedup is achieved within power and noise constraints. Then, we obtain a high-performance and low-power domino logic which is reliable under various noises.

5 Experiment Results

To simplify the analysis, technology mapping is carried out to map the logic to a library which contains NAND gates and NOR gates. For domino logic realization, all the internal inverters are eliminated by using duplication technique.

In this experiment, only 4:1 P:N ratio output inverter is considered since extremely high-skew output inverter is much more susceptible to coupling noise as mentioned Section 3.2. We assume that all domino logic gates are evaluated in standby mode. Thus, leakage currents for each logic gate type are almost same as shown in Figure 7. Table 2 shows experimental results on ISCAS85 benchmark circuits. t_E- denotes critical path speed-up and $P_{act}+$ denotes total active power overhead. All the values shown in Table 2 are delay reduction and power increase percentages

Table 2. Power saving for ISCAS85 benchmark circuits

Circuit	Gates	1% power constraint		2% power constraint		3% power constraint		max power overhead	
		t_E -	P_{act} +	t_E -	P_{act} +	t_E -	P_{act} +	t_E -	P_{act} +
C432	171	9.78%	1.00%	12.50%	2.00%	14.57%	3.00%	**15.91%**	**3.27%**
C880	376	15.37%	1.00%	**18.62%**	**1.76%**	18.62%	1.76%	18.62%	1.76%
C1355	669	9.13%	1.00%	9.59%	2.00%	10.97%	3.00%	**17.33%**	**7.01%**
C1908	550	16.04%	1.00%	18.09%	2.00%	**18.42%**	**2.04%**	18.42%	2.04%
C2670	953	**17.67%**	**0.52%**	17.67%	0.52%	17.67%	0.52%	17.67%	0.52%
C3540	1492	**18.01%**	**0.62%**	18.01%	0.62%	18.01%	0.62%	18.01%	0.62%
C5315	2133	**18.45%**	**0.55%**	18.45%	0.55%	18.45%	0.55%	18.45%	0.55%
C6288	4588	**17.20%**	**0.38%**	17.20%	0.38%	17.20%	0.38%	17.20%	0.38%
C7552	3048	**18.09%**	**0.43%**	18.09%	0.43%	18.09%	0.43%	18.09%	0.43%

with respect to the initial circuits. Initially, all circuits are HH type. For each candidate gate, the optimal size of the keeper transistor is determined to meet the noise constraint mentioned in Section 2.1.

Bold numbers show that the maximum speed-up for each benchmark circuit and active power overhead. Maximum speed up ranges from 15.91% to 18.62% with 0.38% to 7.01% active power increase. Half of benchmark circuits achieve around 18% speed-up with less than 1% active power increase. The average maximum speed up is 17.43% with 1.84% average active power increase. As we can see in Figure 5, the evaluation times of LL type 2-input NAND gate and LL type 8-input OR gate are improved by 20% and 15% compared with those of HH type. Thus, the performance improvement in our results is quite close to the maximum feasible speedup one can achieve with all low V_t configuration. The dual threshold voltage domino logic synthesis method provides such a significant speedup with negligible active power overhead, while maintaining noise margin by appropriate keeper sizing.

6 Conclusion

Domino logic has better performance characteristics than static logic. However, domino logic is much more sensitive to noise. The significant I_{sub} of low V_t transistors in dual V_t technology makes domino logic more susceptible to the noise. Thus, the keeper has to be carefully up-sized to meet the noise constraint when low V_t is applied to domino logic to reduce the critical path delay. The keeper size affects evaluation time, power consumption in active mode and leakage current in standby mode. Furthermore, logic gate types determine the order of the application of low V_t. We have compared possible combinations of transistors equipped with either high or low threshold voltage and suggested dual V_t domino logic synthesis for high performance with noise and power constraint. ISCAS85 benchmark results show that performance is improved by 17% on average, which is significant because the maximum speedup one can achieve with low V_t transistors is about 20%. Another notable result is the negligible power overhead, while noise margin is maintained by keeper sizing.

References

[1] M. W. Allam, M. H. Anis, and M. I. Elmasry. High-Speed Dynamic Logic Styles for Scaled-Down CMOS and MTCMOS Thechnologies. In *Proc. Int. Symp. Low Power Electronics and Design*, pages 155–160, 2000.

[2] A. Alvandpour, P. Larsson-Edefors, and C. Svensson. A Leakage-Tolerant Multi-Phase Keeper for Wide Domino Circuits. In *Proc. IEEE Int. Conf. Electronics, Circuits and Systems*, pages 209–212, 1999.

[3] S. M. Kang and Y. Leblebici. *CMOS Digital Integrated Circuits: Analysis and Design*. McGraw-Hill, 2nd ed., 1998.

[4] J. Kao. Dual Threshold Voltage Domino Logic. In *Proc. European Solid-State Circuits Conf.*, pages 118–121, 1999.

[5] J. Silverman, N. Aoki, D. Boerstler, J. L. Burns, S. Dhong, A. Essbaum, U. Ghoshal, D. H. P. Hofstee, K. T. Lee, D. Meltzer, N. Hung, K. Nowka, S. Posluszny, O. Takahashi, I. Vo, and B. Zoric. A 1.0-GHz Single-Issue 64-bit PowerPC Integer Processor. *IEEE J. Solid State Circuits*, 33(11):1600–1608, Nov. 1998.

[6] S. Sirichotiyakul, T. Edwards, C. Oh, J. Zuo, A. Dharchoudhury, R. Panda, and D. Blaauw. Stand-by Power Minimization through Simultaneous Threshold Voltage Selection and Circuit Sizing. In *Proc. ACM/IEEE Design Automation Conf.*, pages 436–441, 1999.

[7] V. Sundararajan and K. K. Parhi. Low Power Synthesis of Dual Threshold Voltage CMOS VLSI Circuits. In *Proc. Int. Symp. Low Power Electronics and Design*, pages 139–144, 1999.

[8] S. Thompson, I. Young, J. Greason, and M. Bohr. Dual Threshold Voltages and Substrate Bias : Keys to High Performance, Low Power, 0.1um Logic Designs. In *Proc. IEEE Int. Symp. VLSI Technology*, pages 69–70, 1997.