Embedded Robustness IPs

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Abstract: *Due to the VDSM evolution and an electronic systems market starving for performance, the semiconductor industry is used to hit big technology walls. Challenge after challenge, brand new domains of competencies are popping up followed by fast and accurate tools. Synthesis, routers, verification, DFT, embedded systems, SoC, …are well established as standard competencies to achieve high quality, high performance and high yield chip production.*
In recent roadmaps (ITRS, Medea, D&T), signal integrity has been pointed out as a major challenge. More and more causes can affect signal integrity as geometries are shrinking. One of the growing effects is the so-called "transient errors" which are due to temporary condition of use and environment. Cross-coupling, ground bounce, external terrestrial radiations create more and more unpredictable transient and soft errors which affect system reliability in unacceptable ways.
In addition, reliability in devices like memories become a critical issue: the MTBF (mean time before failure) level decreasing the global system FIT (Failure in Time) rate approaching the critical border line for the end user.
Hence, for memories and for logic blocks as well using high-end process technologies, self-correcting intelligence embedded in SoC is needed to enable electronic systems to react against unpredictable and insidious errors.

Main contributing factors

Main contributing factors to transient errors sensitivity are:

1. The decrease of the amount of electrical charge constituting data stored in memory cells due to the decrease of supply voltages and device geometries.
2. Because of the increased density, interconnects on the chip get closer increasing the amount of coupling between them generally referred to as cross talk.
3. The fast rate of change of switching signals creates ground bounce.
4. The already low voltages available to switching devices on the chip even further reduced by temporary drops.

The practical result of these factors is a shrinking stored charge representing data that is increasingly sensitive to outside disturbances such as cross talk, ground bounce and, most importantly, transient faults generated through the exposure to low levels of terrestrial radiation. All of these influences are ***transient*** affecting or destroying ***"only"*** the data permanently but leaving the devices and the semiconductor material intact.

Minimizing the Cost of Eliminating Transient Errors

Clearly, there exists a number of practical ways to tackle the soft error problem. We can enumerate the following, non-exhaustive, list of approaches to try to cope and live with radiation:

1. Careful processing, packaging and interconnect material selection for a decontamination process.
2. Special basic use of materials such as SOS and SOI.
3. Careful device layout geometry design
4. Fault tolerant methodologies implemented at a high level, as the self-correcting intelligence of the chip.

The advantage of this approach is that designs can not only live with radiation but also with other causes of transient errors. No special processing, no special materials are needed. It remains to be proven that such solutions are cost effective in terms of semiconductor real estate, power dissipation while minimally impacting the performance of a design.

Memory Transient Errors: FIT/ bit

In memories, when and where the particle strikes, the information in the struck memory cell or cells may be flipped to the opposite value of what it was. Thus for memories, once the information stored in a cell is flipped, a soft error has occurred and the challenge here is very clear: Detect and correct errors (possibly multiple errors due to adjacent cells) as cost effectively as possible and without or with the smallest possible performance penalty. In memory specifications, the term "FIT / Mbit" starts to be adopted as a standard to qualify memory reliability and availability. This constraint encompasses more than radiation induced soft errors, but also temperature and humidity conditions, ground bounce sensitivity, drops in voltage…

To reduce the FIT rate to the minimum, standard ECC could be used, but a delay to generate code and to check data and addresses is required, and extra silicon cost as well.
Embedded Robustness IPs thanks to an optimized architecture connected with the rest of the chip enable a reduction of these penalties. In fact, a test chip experienced no performance penalty and only one extra bit was needed to detect and correct single error.

Logic Transient Errors: FIT/Gate

For digital logic, the chain of events from the time when a particle strikes to when data is corrupted due to a soft error or an aggressor signal slowing down a weak signal creating a timing fault is more complex. Simulation tools begin to provide accurate information, and experiment on iRoC test chip shows that the FIT/gate constraint should be taken as seriously as for memories.

Last results on a 32 bit RISC processor and high end memories experiments

Because soft errors are the most accessible transient errors to simulate, to create and to measure their effects on a die, this phenomenon has been simulated on a silicon chip.
In [Nic et. al], the time redundancy concept is described.
This technique is very well adapted to detect transient pulses due to radiation in chips not exceeding 500 MHz with a clock domain pretty homogeneous. Time redundancy enables to detect timing faults due to cross-talk or ground bounce as well with no performance penalty. To avoid the discussed limitations of time redundancy schemes and to spread protection techniques to complex and high-speed chips, other design techniques are available at iRoC Technologies. These techniques are based on ECC for logic. Instead of adding extra latches to compare the signal at two different instances, a specific signature will be processed for independent cones of logic through traditional ECC.
Using time redundacy design methodology, iRoC designed specific embedded Robustness IP, which have been implemented in logic blocks of a 32-bit RISC processor manufactured in a 0.25µm commercial technology.
The radiation test campaign enabled to inject errors inside the die, thanks to ionized particle with a broad range of energy.
The results show key points and question generally accepted ideas. In fact, all soft errors latched have been monitored and a first ever comparison of logic sensitivity and memory sensitivity has been performed.

Particles Energy (MeV)	5.85	14.1	34	55.9
Memory sensitivity Cross Section/ bit	32	37	48	53
Logic sensitivity (40 MHz in experiement) cross section / gate	2.5	4.1	7.1	9
Logic Sensitivity (350 MHz with simulation tool)	23	37	64	81

The most significant conclusion is the fact that under particular conditions, especially using high clock frequencies, logic blocks and memories with comparable quantity of transistors can have the same sensitivity in terms of Soft Error rate.
This tends to proof that for high-end chips a full protection is now mandatory.

A second type of tests is pure static neutron testing on high-end memories. A large spectrum of neutron energy is used to simulate the terrestrial environment, and stresses memories in 0.13 µm technology. As a matter of fact, taking the natural neutron flux at sea level, a FIT (Failure in Time) rate per Mbit can be extrapolated after these accelerated test campaigns.
The results give an average level of 2000 FIT/ Mbit which is the border line of SIA recommendations. In fact, with this value, Soft Errors could affect some systems every 2 weeks.

Conclusion:

Transient errors encompass multiple effects, which affect more and more the integrity of operation electronic systems using high-end and fast chips. Compared to permanent errors, tackled with DFT, ATE, ATPG, transient errors are particularly insidious because they are unpredictable, and undetectable errors causing system crashes without specific mechanisms inside. Soft Errors are a part of this challenge, and to simulate them ease the understanding of the chip reaction under stress or unusual operating conditions. These first RISC processor tests using iRoC IPs experience that “Embedded Robustness IPs” seem to be the control panel and the reliability insurance for a broad range of transient errors adding a minimum extra cost with no performance penalty.

References:

[NIC 99] M. NICOLAIDIS, "Time Redundancy Based Soft-Error Tolerance to Rescue Nanometer Technologies", in proceedings VTS.