Analog IP testing: Diagnosis and Optimization

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Abstract

In this paper, we present an innovative methodology to estimate and improve the quality of analog and mixed-signal circuit testing. We first detect and reduce the redundancy in the electrical test measurements (e-tests), then we identify the e-test acceptability regions by considering performance specifications as well as process parameter distributions. Finally, we provide an effective metric for the accurate assessment of the parametric test coverage of embedded analog IP. Experimental results confirm the validity of the proposed methodology and its broad applicability to analog, mixed-signal and RF applications for different process technologies.

1. Introduction

Testing analog functions is expensive and difficult. Unlike the case for digital circuits, where signal observability and controllability is achieved by means of suitable Design For Testability techniques and efficient test programs can be automatically generated by logic synthesis tools, analog test development still requires careful manual optimization and efficient interactions between circuit designer, process and test development engineers. In the digital testing domain easy fault models such as "stuck at" faults, which stem from the dominance of functional limited yield loss (shorts and opens) mechanisms, can be applied. Nevertheless, parametric faults are at least as important as random and systematic defects in mixed signal applications. Therefore, simplified models for the detection of catastrophic faults may not be adequate. These problems are exacerbated by the difficulty of adding additional components to achieve controllability and observability of analog nodes without significantly perturbing their impedance and, in turn, the performance of the block under test. Finally, analog testing is usually more expensive, both in terms of equipment cost and testing time because it requires more sophisticated equipment and time consuming parametric tests.

In this work, we present a methodology which addresses the issue of analog testability by using statistical models of embedded analog core performance parameter variability as functions of a set of simple electrical test (e-tests) measurements. The use of e-tests as Process Control Monitors (PCM) at wafer sort to scrap low or zero yielding wafers before expensive functional and parametric tests is well known [1][2][3][4][5][6]. However, unless a great deal of attention is dedicated in the development and refinement of an appropriate suite of e-tests, they may not correlate well with actual performance of the analog cores. At the same time, a significant amount of e-test redundancy may cause unnecessarily long testing time. This is often due to two different causes. E-tests do not measure independent phenomena and they are typically designed to guarantee the range of device parameter variation described by SPICE corner models rather than considering their statistical correlation with the circuit performance parameters. As such, they are not sufficient to guarantee satisfactory test coverage for a particular analog core. In this work we also address e-test redundancy elimination by using a set of well known statistical techniques such as Principal Component Analysis [7][8] (PCA). We also present a technique to assess and improve the quality of test coverage achieved by a given set of e-tests relative to a pre-defined set of analog core performance targets. We assume that a circuit fault occurs if at least one of the performance constraints is violated and, as in [6], satisfaction of the specifications can be inferred directly from the measurements. However, the validation criteria in [6] exploit posterior probabilities extracted from a training data set to classify the circuit with respect to one given specification, while our methodology allows to directly verify specification compliance, by simply evaluating quadratic performance macromodels. Finally, the proposed test coverage metric differs from the work presented in [9], because we locate performance values in the variability space and thus automatically verify their belonging to the acceptability region/hyperspace defined by performance specifications.

The paper is organized as follows. We present the mathematical foundations and the major steps of the methodology in Section 2. The metric adopted for the parametric test coverage estimation is described in Section 3. The analysis of experimental results is reported in Section 4.

2. Description of the Methodology

2.1. Replacement of Basic Process Factors

Let us assume that the analog core to be tested is composed of a finite number of sub-circuits, (c_i, $i = 1, \ldots, N_c$). Each of the design sub-circuits can be accurately simulated in a reasonable time with SPICE. Examples of analog cores and associated sub-circuits are shown in Table I.

Analog Core	Sub-circuits	Performance
PLL	Phase Detector	resolution, speed
	Loop Filter	phase noise, linearity
	VCO	phase noise, tuning range, linearity, gain
Flash A/D	Voltage Reference	stability
	Comparators	speed
	Decoder	speed

TABLE I: Analog core examples

The sub-system functionality is completely specified in terms of a set of performance parameters ($y_{j,\ j\ =\ 1,\ \ldots,\ N_y}$), and each of the y_j can be accurately estimated by simulating one of the sub-blocks c_i. Examples of such performance parameters are also shown in Table I.

Let us call $m_{l,\ l\ =\ 1,\ \ldots,\ N_m}$ the set of PCM data that are measured at wafer or die sort. Each e-test can also be accurately simulated by using SPICE. Typical analog test monitors are V_{TH}, I_{dsat}, g_m for MOSFET devices and H_{FE} and R_{bb} for BJT devices. Finally, let us assume that the entire variability of the manufacturing process can be captured by using a set of parameters which can be modeled with a set of uncorrelated random variables $x_{k,\ k\ =\ 1,\ \ldots,\ N_x}$ with zero mean and unit variance, which we will call process factors.

The relation between the electrical characteristics of transistors and passive components, including wiring parasitics, and process factors, can be accurately captured by generalized statistical SPICE models, which express all the relevant functional and statistical dependence between every SPICE model parameter and a subset of the process factors, also including parameter to parameter and intra-die correlation information. In addition to traditional statistical SPICE models, like those described in [1],[10],[11],[12] the process factors x_k account for back end of line variations, such as metal layer thickness, inter-layer dielectric thickness,via resistivity, etc.

The first step of our method is to use Response Surface Methodology[13] (RSM) and SPICE to create low order, multi-variate polynomial models of every circuit performance parameter y_j and every PCM measurement m_l as functions of the process factors, namely:

$$\begin{aligned} y_j &= y_j(x_1, \ldots, x_{N_x}),\ j\ =\ 1, \ldots, N_y \\ m_l &= m_l(x_1, \ldots, x_{N_x}),\ l\ =\ 1, \ldots, N_m \end{aligned} \tag{1}$$

The observed variations of the PCM measurements m_l can be used to predict the variability in the circuit performance parameters y_j; however, some of the circuit performance parameters may be sensitive to the variation of process factors that is not actually sensitized by any of the current PCM measurements. Nevertheless, there could also be the case where the PCM measurements are sensitive to process factors not relevant for the circuit performance characterization. Moreover, PCM measurements are not independent, hence some of them are partially redundant statistical estimators of the circuit performance variability [14][15][16].

Let $\Xi_y(x) \subseteq \Re^n$ and $\Xi_m(x) \subseteq \Re^m$ be the co-domain of the mapping from circuit performance parameters and PCM measurements respectively, belonging to the process factor space $X \subseteq \Re^k$. Then, let us denote the cardinality of the performance and the e-test set by N_y and N_m, respectively. The above limitations can be expressed in terms of the following properties:

$$\begin{aligned} &(i) \quad n \neq m \\ &(ii)\ N_m > m \end{aligned} \tag{2}$$

Property (i) expresses the fact that the circuit performance parameters are sensitive to a different number of independent process factors than those that are sensitized by the PCM measurements, while property (ii) is a consequence of the fact that the PCM measurements are not linearly independent, hence $\Xi_m(x) \subseteq \Re^k$.

In order to identify a basis in the PCM space, we apply a Principal Component Transformation to the PCM variables, i.e. an orthonormal transformation such that:

$$\begin{aligned} e = \Gamma^T m,\ \Gamma^T\Gamma\ =\ 1, \\ \Gamma^T Cov(m)\Gamma\ =\ \Lambda \end{aligned} \tag{3}$$

where Λ is diagonal and $\lambda_{i,\ i} \geq \lambda_{j,\ j}$ for $i < j$.

It is possible to show that the transformed variables, also called Principal Components (PCe) in the e-test space, are linearly independent and that no other linear combination of the original variables has variance greater than $\Lambda_{1,\ 1}$. By substituting (3) in (1), and assuming a linear dependence between e-tests and process factors, i.e. $m\ =\ Ax$, we obtain:

$$e\ =\ (\Gamma^T A)x \tag{4}$$

The adoption of linear models to describe the e-tests as a function of the process factors is mandatory to guarantee the existence of the inverse function. It should be noted that the assumption of linearity, limited to the e-tests set, can be consider of general validity, as confirmed by the experimental results, however there may be sporadic cases where this linear approximation is not completely satisfactory.

Since the e variables are uncorrelated, it can be proven

that the rows $\Gamma^T A$ are linearly independent, and if $e \in \Re^{N_e}$ with $N_e \le N_x$, then $rank(\Gamma^T A) = N_e$.

Proof: If a_i and a_j are the i-th and j-th rows of $(\Gamma^T A)$, with $i \neq j$ and $x_{k,\, k = 1,\, \ldots,\, N_x}$ are process factors, then: $(a_i \cdot a_j) = \sum_k a_{ik} a_{jk} =$

$$\sum_{k=1}^{N_x} a_{ik} a_{jk} \cdot E x_k^2 = E(a_i x a_j x) = E(e_i e_j) = 0$$

which shows that the rows of $\Gamma^T A$ are linearly independent.

Now, we need to consider three different cases. If $N_e = N_x$ then $\Gamma^T A$ is a full rank square matrix that can be inverted. Otherwise $\Gamma^T A$ is a rectangular matrix and the system can be overdetermined $(N_e > N_x)$ or under determined $(N_e < N_x)$. When the cardinality of PCe is larger than the number of process factors, we simply drop the last $N_e - N_x$ rows of $\Gamma^T A$, i.e. the $N_e - N_x$ least significant PCe, obtaining a full rank invertible square matrix. In the case that, $N_e < N_x$, and thus $rank(\Gamma^T A) = N_e$, there are exactly $N_x - N_e$ free variables, and the matrix $\Gamma^T A$ can be reduced in echelon form by gaussian elimination, or LU factorization, yielding:

$$Ux = L^{-1} Pe, \text{ with } LU = \mathrm{P}\Gamma^T A \tag{5}$$

where P is a suitable permutation matrix.

It is possible to change the position of the N_e rows which contain the N_e pivots associated with the N_e basic variables by choosing a different permutation matrix; the remaining variables are free variables [17]. The general solution of this under determined system $Ux = L^{-1} Pe$ is the sum of one particular solution, obtained by setting all the free variables to zero , and a homogeneous solution, computed by choosing the $N_x - N_e$ free variables as independent parameters. Another procedure for identifying the N_e of the most significant process factors consists on factoring the original matrix $\Gamma^T A$ by applying a singular value decomposition [17], namely:

$$\Gamma^T A = S \Sigma V^T \tag{6}$$

where the columns of S and V^T include the eigenvectors of $(\Gamma^T A)(\Gamma^T A)^T$ and $(\Gamma^T A)^T(\Gamma^T A)$, respectively, while Σ is a diagonal matrix containing the square roots of the eigenvalues of both $(\Gamma^T A)(\Gamma^T A)^T$ and $(\Gamma^T A)^T(\Gamma^T A)$. In this case, the subset of N_e process factors with dominant eigenvalues can be identified by applying a QR decomposition to the matrix V^T.

2.2. Circuit Performance Evaluation

As mentioned in the previous section, it is possible to express circuit performance targets as a function of process factors. However, since process factors can be replaced by a linear combination of principal components in the e-test space, we are able to accurately evaluate the selected circuit performance by exploiting simpler e-test measurements.

We implemented two different methods of evaluating the statistics of the performance targets. In the simplest one, we first combine the following equations:

$$\begin{aligned} y_j &= y_j(x_1, \ldots, x_{N_x}),\ j = 1, \ldots, N_y \\ x_k &= x_k(e_1, \ldots, e_{N_e}),\ k = 1, \ldots, N_x \end{aligned} \tag{7}$$

to obtain the linear/quadratic performance macromodels as a function of independent e-tests, namely:

$$y_j = y_j(e_1, \ldots, e_{N_e}),\ j = 1, \ldots, N_y \tag{8}$$

Thus, the statistical characterization of the performance can be carried out by simply plugging the values of the e-test measurements into (8). The availability of these macromodels allows knowing if the circuit performance values associated with a generic set of e-tests, fall in the acceptability region or not. Therefore faulty circuits can be discarded on then basis of this criterion.

The more complex approach for estimating circuit performance data consists of re-simulating circuits using e-test based models (E models), instead of statistical models which rely on independent process factors (X models). However, this verification can be cumbersome from the computational standpoint, since it requires running a Design of Experiments[18] (DOE) with as many independent variables as the global number of e-tests associated with all the devices included in the circuit. However, an appropriate screening of the input variables can be done (i) by simply running a simplified DOE and examining the sensitivity of the circuit performance functions with respect to different e-tests or (ii) by considering the normalized values of the coefficients of the macromodels.

3. Parametric Test Coverage Assessment

Fault coverage for analog circuits cannot be restricted to potential shorts and opens which can be easily detected by a test, since parametric faults spanning a continuous range of circuit element variations are likely to occur and also harder

to detect [9]. Moreover, discarding a circuit due to an 'out-of-range' element value which actually does not threaten specification compliance can significantly reduce yield. Therefore, only a statistically-based definition of the Figures of Merit of the circuit (FOMs) in terms of e-test measurements can provide an accurate analog test metric. Performance constraints are usually coincident with the specifications for the application to be developed. Therefore, circuits that do not meet performance requirements are considered as faulty and then discarded.

In order to provide an accurate assessment of the parametric test coverage offered by a set of e-test measurements, we need to know the actual circuit performances. Nevertheless, if the set of process factors describes the entire variability of the performance parameters, it is realistic to assume that the performance values obtained by simulating the X models adequately represent the real case.

The definition of the test coverage metric can be easily interpreted by looking at the diagram depicted in Fig. 1. The circles and the squares represent performance values obtained with X and E models, respectively, while the shaded area indicates the Acceptability Region (AR) of the circuit performances.

There are four possible cases:

(a) Both X and E belong to AR.

(b) Neither X nor E belong to AR.

(c) X, but not E belongs to AR.

(d) E, but not X belongs to AR.

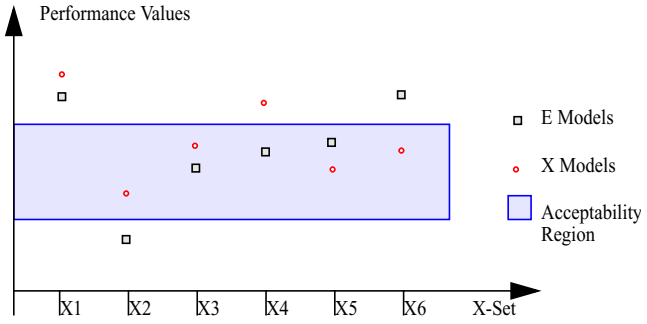

Fig. 1. Representation of the circuit performance space.

The test coverage can be defined as the ratio between the number of runs where both X and E models present the same behavior over the total number of runs:

$$\frac{(a+b)}{(a+b+c+d)} \tag{9}$$

As a matter of fact, in case (a), we keep a circuit which works correctly, while in case (b) we reject a faulty circuit.

4. Experimental Results

The proposed methodology has been applied to a SiGe-BiCMOS process with minimum feature size of 0.25 μm, however its general validity allows for extension to different process technologies and/or circuit applications. First, the existing set of e-tests has been simulated for each device present in the circuit using X models. After extracting the RSM models of the e-tests, each process factor has been replaced by a linear combination of independent e-tests in the so-called E models. The linear models of the e-tests as a function of the process factors has guaranteed an accuracy higher than 98% in fitting all of the e-test measurements as confirmed by the Circuit Surfer [19] statistical simulation and optimization tool used to characterize the e-tests and circuit Figure Of Merits (FOM). To verify the validity of the methodology, the initial e-tests have been resimulated using E and X models. The comparison of the e-test statistics obtained by simulating these two different models has been-carried out on the basis of a Monte Carlo experiment with 1000 samples.

E-tests	Mean	Stdev
e-test 1	0.23%	0.42%
e-test 2	0.11%	-2.00%
e-test 3	0.16%	-2.24%
e-test 4	0.22%	-3.75%
e-test 5	0.10%	-1.70%
e-test 6	0.08%	-2.11%
e-test 7	0.11%	-1.98%
e-test 8	0.15%	-2.23%
e-test 9	0.23%	-3.71%
e-test 10	0.10%	-1.69%
e-test 11	0.08%	-2.10%
e-test 12	0.00%	-5.14%
e-test 13	0.00%	-3.82%

TABLE II: Comparison of e-tests statistics

In Table II, we report the percentage error on mean and standard deviation that is committed when E models are applied in place of the original ones. Results confirm that the process factors can be replaced by a non-redundant set of e-tests without losing information in terms of the variability of the e-test themselves.

For the FOM's evaluation, first a DOE has been applied to obtain a quadratic RSM of the performance ($y_{j,\ j\ =\ 1,\ \ldots,\ N_y}$) of a generic circuit as a function of process factors $x_{k,\ k\ =\ 1,\ \ldots,\ N_x}$. Then a 10000 samples Monte Carlo experiment have been run in Circuit Surfer to obtain a significant run set. On the other hand, the simulation of the e-tests described above has allowed for the extraction of the linear relationship between $x_{k,\ k\ =\ 1,\ \ldots,\ N_x}$ and E. The replacement of the Xs with the Es in the original RSMs provides a quadratic models of circuit performance as a func-

tion of independent e-tests. The statistics of the original runtable have been compared with the statistics of the values obtained by evaluating the performance macromodels for different RF circuits, such as for example a LNA for CDMA applications. Results are summarized in Table III. Obviously, this approach presents a general validity since there are no constraints in terms of topology, size, etc. on the circuits that can be tested. Finally the parametric test coverage evaluation, described in Section 3, has been applied by imposing an acceptable variation of 3 sigma on the FOMs and the results are reported in Table IV.

CKT/PERF	Model	Mean	Stdev	Err. Mean	Err. Stdev
LNA Gain	X-mod	18.73	0.56	-0.02%	-1.47%
	E-mod	18.726	0.551		
LNA IIP3	X-mod	-10.2	0.833	0.01%	-1.97%
	E-mod	-10.201	0.815		
LNA Noise Figure	X-mod	0.8935	0.043	-0.05%	-1.19%
	E-mod	0.8931	0.042		
Mixer Gain	X-mod	8.823	0.1236	0.03%	-3.21%
	E-mod	8.825	0.1197		
Mixer IIP3	X-mod	-5.428	0.4069	0.06%	-0.13%
	E-mod	-5.431	0.4063		
Driver Gain	X-mod	12.75	0.0493	-0.03%	0.65%
	E-mod	12.745	0.0496		
Driver OIP3	X-mod	27.9	0.8377	-0.01%	-0.60%
	E-mod	27.89	0.8332		
VCO Phase Noise, 50KHz	X-mod	-95.57	0.1527	0.00%	0.39%
	E-mod	-95.57	0.1533		
VCO Phase Noise, 1MHz	X-mod	-121.8	0.1566	0.03%	0.34%
	E-mod	-121.83	0.1571		

TABLE III: Comparison of circuit performance statistics

5. Conclusion

In this paper, we presented an efficient technique to assess the quality of analog and mixed-signal test, which is not limited by the application or process technology. After eliminating redundant e-test measurements, we were able to map the acceptable range of variability of the measurements directly in the analog circuit performance space. An accurate metric was derived for calculating the parametric test coverage given by a set of e-tests, assuming that the underlying statistical SPICE models capture all the relevant process variability.

CKT/PERF	Test Coverage
LNA Gain	98.9%
LNA IIP3	99.6%
LNA Noise Figure	98.8%
Mixer Gain	99.1%
Mixer IIP3	98.6%
Driver Gain	99.3%
Driver OIP3	99%
VCO Phase Noise 50KHz	99.5%
VCO Phase Noise 1MHz	99.3%

TABLE IV: Parametric test coverage

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