# Sizing Power/Ground Meshes for Clocking and Computing Circuit Components

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**Abstract**

*This paper presents a new formulation and an efficient solution of the power and ground mesh sizing problem. We use the key observations that (1) the drops in power and ground node potentials are due not only to currents drawn by the computing blocks, but also to those drawn by the clock buffers, and (2) changes of circuit component delays are linearly proportional to the power/ground IR-drops. This leads to a linear quantification of the timing relations between the clocking and computing components in terms of the power/ground IR-drops. Our method removes all IR-drop related timing violations that occur in about 2% of paths when grids are sized using the existing methods that satisfy the maximum IR-drop constraints. In addition, we achieve supply mesh area improvements of the order of 30% while simultaneously reducing the power dissipated in the circuits by about 6.6% compared to traditional grid sizing methods.*

## 1. Introduction

Traditional power/ground (p/g) mesh sizing minimizes the grid areas in order to satisfy electromigration, design rule, and node potential drop constraints. The node potentials are computed by considering currents drawn by the computing blocks only, not the additional voltage drops caused by currents drawn by the clock buffers. Since changes in the p/g node potentials affect both the clocking and computing components in the circuits, timing closure in presence of p/g IR-drops can be achieved only if the additional temporal constraints in the computing paths are satisfied. In order to generate these constraints, there needs to be a relation between the p/g IR-drops and the delays induced thereby in the clocking and computing components. In this paper we use the linear relations between delays of active components and the p/g IR-drops derived in [8], incorporate timing constraints into our linear programming based mesh sizing formulation, besides the other constraints in traditional methods, and solve them efficiently. Existing methods do not guarantee timing robustness, which is often loosely justified as a side-effect of restricting the p/g node potential drops. Besides achieving area and power improvements compared to meshes designed by traditional methods, our algorithm generates timing-safe supply meshes with limits of maximum potential drops similar to those obtained by existing methods. However, the distribution of node potentials within this bound is more uniform in our meshes. Our method tends to reduce the operating potential differences across a greater number of transistors than do existing methods. Hence it slows down transistor aging effects and leads to more reliable circuits.

In figure 1 we show a sub-circuit consisting of two clocked blocks *i* and *j*, a clock buffer, and a portion of a supply grid. These blocks could be IP Cores. We assume that timing relations inside these blocks are satisfied. The input signal from the block *i* arrives at the input of *j* at time $t_{ij}$. The delay of the clock-input of *j* with respect to the clock source is $\delta_j$. Assume that all active elements inside a mesh square are supplied by the same mesh node as shown by the bold dashed lines in the figure.

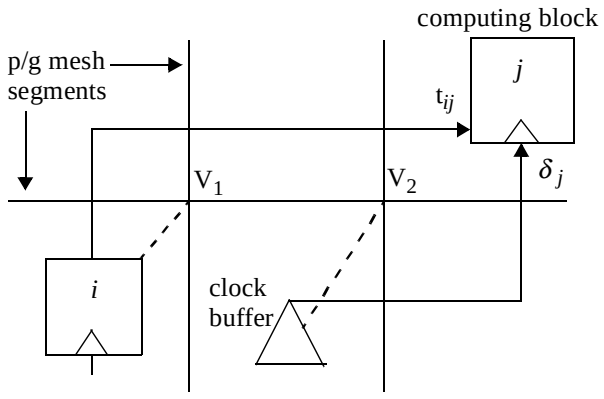



**Figure 1: Portion of a typical circuit layout**

Due to the resistive nature of the supply grid, the potentials $V_1$ and $V_2$ may deviate from ideal values. Figure 2 shows an IR-drop-induced timing violation. $\Delta t_{ij}$ is the

change in the arrival time of the signal from the block *i* at the input of *j* due to IR-drops in the supply nodes $V_1$ and $V_2$. Similarly the IR-drop-induced change in delay of the *j* clock-input with respect to the clock source is $\Delta\delta_j$. The input timing constraint for *j* is satisfied for the case with no IR-drops (figure 2(a)). Non-zero IR-drops in the supply nodes $V_1$ and $V_2$ may give rise to the scenario in figure 2(b) when set-up time violation occurs (equation c in figure 2), even though the maximum change of potential constraints (equations a and b in figure 2) have been satisfied.

We assume that a placed and interconnected circuit of synchronous computing blocks and a clock-network are given. On this we have superimposed p/g meshes for supplying both the clock-network and the computing logic. The aim is to size the given p/g meshes to achieve correct timing and functionality in the presence of p/g IR-drops while satisfying design rule, electromigration, and maximum IR-drop constraints. In our method, the IR-drop constraints are required to bound the supply voltages of the active devices to ranges within which their delays change linearly with the fluctuations in the their supply potentials.

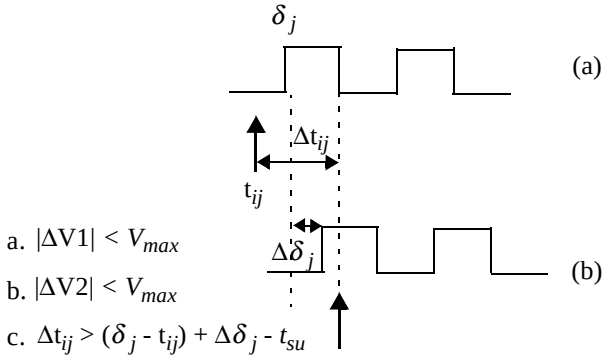



**Figure 2: Timing relations between signal and clock**

Power/ground grid sizing with resistive mesh segments is known to be a constrained nonlinear optimization problem and has been fairly well studied [2],[3],[4]. In [2] resistance and branch currents are treated independently, which results in non-linear cost function and constraints. The Lagrangian method solves this problem using the steepest descent algorithm. In the existing literature there are two other approaches: a gradient based approach that has a linear cost function but non-linear constraints [4], and one that solves a sequence of linear programs [7]. In the latter method, the optimization problem is solved iteratively in 2 phases. First all branch currents are fixed, which leads to a convex programming problem solved by the conjugate gradient method. The second phase leads to a linear programming problem with fixed nodal voltages. It is well known that the method in [7] achieves faster convergence and better results. A sequence of linear programs always converges to the optimum solution of the relaxed convex problem. In [5] the authors observe the relation between IR-drops in the p/g meshes and its effect on slowing down the critical paths in the circuit and changing clock skews. They present a methodology to analyze the resulting signal integrity issues, but do not attempt optimization of the supply networks, the clock network, or the logic elements to achieve timing closure.

The effect of p/g IR-drops on clock skew was experimentally observed in [6]. However, it was a simulation and verification based work, which did not try to optimize the p/g networks to meet timing in the presence of IR-drops.

In the next section we discuss the expressions which establish the linear dependence of delays on the p/g IR-drops, and support our results with experimental evidence. In section 3 we perform a timing analysis of the circuits having interconnected synchronous blocks, and derive linear timing constraints that are IR-drop dependent. The problem is formally stated in section 4 with a discussion of the solution algorithm that we adopt. In section 5 we describe our experimental set-up, benchmarks and the basic design flow. Results are presented and analyzed in section 6. We draw conclusions in section 7, and state our current and future research directions.

## 2. Buffer delay change - a linear function of p/g IR-drops

A simple closed-form formula has been developed in [8] to estimate the buffer delay change in presence of the p/g noise. A buffer is a chain of tapered inverters. These results were derived using the short-channel MOSFET model which considers carrier velocity saturation effects. Since the formulas are general and independent of circuit structure, linear relations exist between the change of delay of any active circuit element and its supply IR-drops.

We use $V_{dd}$ and $V_{ss}$ to denote the ideal power and ground levels when there is no noise ($V_{ss} = 0$). In presence of power and ground noise, we use $\Delta V_{dd}$ and $\Delta V_{ss}$ to represent the variation of power and ground levels respectively. In other words,

$$\Delta V_{dd} = V'_{dd} - V_{dd} \text{ (power noise)}$$

$$\Delta V_{ss} = V'_{ss} - V_{ss} = V'_{ss} \ (V_{ss} = 0) \text{ (ground noise)}$$

The derivations in [8] show that the incremental change of buffer delay induced by power and ground variations for the falling transition, ($\Delta t_{pHL}$), can be expressed by the following equation:

$$\Delta t_{pHL} = f_1 \cdot (\Delta V_{ss} + \Delta V_{dd}) - f_2 \cdot (\Delta V_{dd} - \Delta V_{ss}) \qquad (1)$$

where $f_1$ and $f_2$ are constants dependent on input transition time, gate load, and the device and technology parameters. The expressions for $f_1$ and $f_2$ have been theoretically derived

in [8], and are not shown here. We have similar equations for logic low to high transition through the p-MOSFET of an inverter, $\Delta t_{pLH}$. The main difference is that the parameters of the coefficients $f_1$ and $f_2$ are obtained from the corresponding p-MOSFET. Hence, the average change of buffer delay is:

$$\Delta T_d = \frac{\Delta t_{pHL} + \Delta t_{pLH}}{2} \qquad (2)$$

Equation (1) can be explained by observing that the voltage difference between the power supply and ground levels determines how fast a gate charges or discharges its capacitive load. This in turn affects the delay and the transition times of the gate output. The larger the difference ($\Delta V_{dd}$ - $\Delta V_{ss}$), the faster the gate output switches, and hence the smaller the output delay. The quantity ($\Delta V_{dd}$ + $\Delta V_{ss}$) affects the switching threshold of the gate, and an increase in its value increases the threshold voltage. A higher value for the gate threshold implies an increase in the gate delay. Note that for a purely resistive network, $\Delta V_{ss}$ will always be positive and $\Delta V_{dd}$ will always be negative.

HSPICE simulation results in [8] experimentally corroborate the linear dependence of change of delay ($\Delta t_{pHL}$) of a buffer on the p/g IR-drops in the 0.25 µm technology ($V_{dd}$ = 2.5V). These results are shown in figure 3 (a,b). Note that $\Delta t_{pHL} = 0$ for $\Delta V_{dd} = \Delta V_{ss} = 0$.

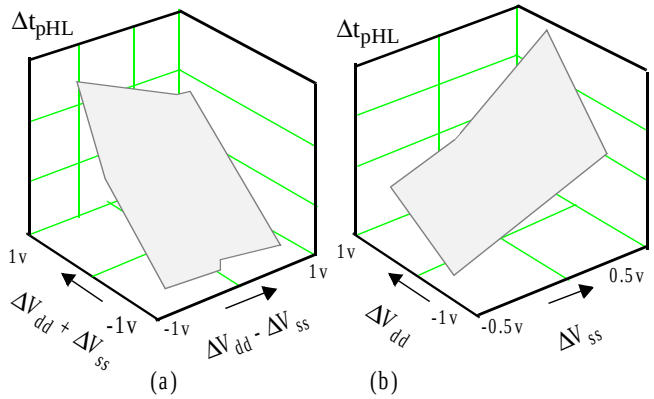



**Figure 3:**
**Change of delay varies linearly with p/g IR-drops**

Note that the plots are linear in most areas except the edges. The amount of noise in the supply lines at the edges vary from +1 volt to -1 volt, which is 80% of the ideal $V_{dd}$. Such huge supply line noises are not practically tolerated either way. Thus, our delay change-supply noise model is accurate up to the presence of considerable amounts of supply noise. In our experiments we have limited the maximum IR-drop at any p/g node to 10% of the ideal value. Within these bounds, we have experimentally observed that the delays of the active devices in our circuits change linearly with IR-drops.

A necessary condition for the linear dependence of delay on p/g IR-drops is the equality of all rise and fall transition times at the inputs and outputs of the inverters forming a buffer. In this work all the buffers are taper-designed so that the above condition is valid, and as shown in figure 4, $t_{r1} = t_{f2} = t_{r3}$. Thus the following condition must be satisfied:

$I/\beta C = \beta I/C_L$ or $\beta = \sqrt{C_L/C}$. Here β is a coefficient greater than 1.

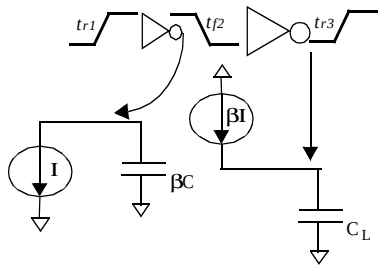
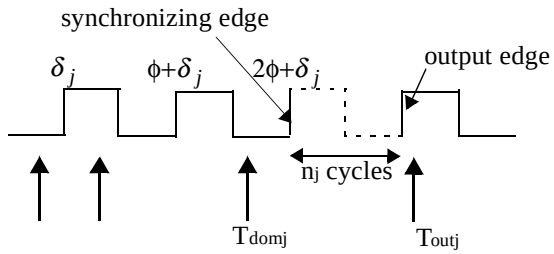



**Figure 4: Small signal inverter models**

## 3. Timing Analysis




$\delta_j$ : clock signal arrival time

**Figure 5: Timing diagram of a block**

The arrival times of the inputs to a block *j* are shown in figure 5. The clock period is ϕ. A dominant input is the one to which the block's output evaluation time is sensitive. The arrival time of the dominant input is shown as $T_{domj}$ in the figure. If it takes $n_j$ clock cycles for the block's output to be ready after that, its output evaluation time will be given by $T_{outj}$:

$$T_{outj} = T_{domj} + n_j\phi \qquad (3)$$

All the inputs (whether arriving within the same clock period or not), must satisfy the timing constraints in the presence of p/g noise. If there are no p/g IR-drops, then for any input *i* to the block *j* arriving at the time $t_{ij}$ between $(n-1)\phi+\delta_j$ and $n\phi+\delta_j$, such that there are no set-up time ($t_{su}$) and hold time ($t_{ho}$) violations, the following relation must be satisfied:

$$(n-1)\phi + \delta_j + t_{ho} \le t_{ij} \le n\phi + \delta_j - t_{su}$$

In the presence of p/g noise, however, the clock signal delay and the arrival time of the input signal will both change. In our formulation we ensure that even in the presence of p/g IR-drops, the changed value of $t_{ij}$ lies between the changed values of $(n-1)\phi+\delta_j$ and $n\phi+\delta_j$. In such a case the following relation has to be satisfied:

$$(n-1)\phi + (\delta_j + \Delta\delta_j) + t_{ho} \le t_{ij} + \Delta t_{ij} \le n\phi + (\delta_j + \Delta\delta_j) - t_{su}$$

Rearranging the above equation and clubbing the constant terms into the constants $C_1$ and $C_2$ ($C_1 < C_2$), we obtain the following simple relation between the changes in the signal and clock arrival times:

$$C_1 + \Delta\delta_j \le \Delta t_{ij} \le C_2 + \Delta\delta_j \qquad (4)$$

***Theorem 1***

In the presence of p/g IR-drops, all the timing relations inside a clocked block can be expressed as constraints on the maximum changes of the supply potentials of the block.

***Proof***

Given a fixed p/g mesh internal to a block, it is possible to formulate an LP problem with timing constraints expressed in terms of the p/g node IR-drops. The cost function would be the total change of potential drop across the block, which should be maximized. If the ground node is assumed ideal, the change of potential drop across the block is due to IR-drop in its power node, and vice-versa. Otherwise, both the nodes contribute to the cost function. The solution to this problem yields the upper bounds of the deviations of the external p/g mesh node potentials from their ideal values, which can be tolerated without violating the original timing relations satisfied under ideal supply conditions.

***Theorem 2***

The change in output evaluation time for a clocked block is equal to the change in the clock arrival time at its clock-input, provided the power/ground node potential drops are bounded.

***Proof***

The potential drops of the p/g mesh nodes can be bounded to values such that no internal timing violations occur according to theorem 1, and equation (4) is satisfied. This ensures that timing-closure is maintained even with p/g noise-induced change of delays, and thus the timing constraints at the input interface of the block will be satisfied. Change in $T_{domi}$ is equal to the change in clock arrival time, since all signals are latched into and out of the block at the rising edge of the clock signal. This is equal to the change of the output evaluation time of the block according to equation (3).

The above theorem establishes the following relation:

$$\Delta T_{outj} = \Delta\delta_j \qquad (5)$$

The input signal arrival time $t_{ij}$ is the output evaluation time of the block $i$ ($T_{outi}$) plus the delay of active elements $D_{ij}$ on the interconnection between $i$ and $j$. If this interconnection is a local wiring, there may not be any active elements on it and $D_{ij}$ will be 0; but for global wiring there may be buffers on the interconnection, and $D_{ij}$ will be non-zero. If the distance between two active elements on an interconnect is short enough so that resistive effects do not dominate, we can use linear superposition to add up the change of delays (caused by p/g noise). Thus, if the total change of all active element delays on the wiring between $i$ and $j$ adds up to $\Delta D_{ij}$, we can express the change of input signal arrival time to $j$ as:

$$C_1 + \Delta\delta_j \le \Delta T_{outi} + \Delta D_{ij} \le C_2 + \Delta\delta_j$$

Using equation (5), this translates to:

$$C_1 + \Delta\delta_j \le \Delta\delta_i + \Delta D_{ij} \le C_2 + \Delta\delta_j \qquad (6)$$

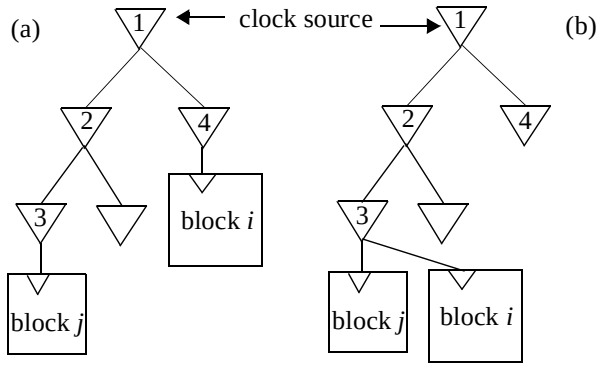



**Figure 6: Clock trees**

In figure 6 (a) we show a portion of a clock tree that drives the blocks $i$ and $j$. The clock input of block $i$ has an ancestor set of clock-tree buffers {1,4} and that of block $j$ is {1,2,3}. Let the change of delays due to p/g IR-drops for each one of these buffers be represented by $\Delta\delta_x$ (x = 1,2,3,4). Analyzing equation (6), we can express $\Delta\delta_i$ as $\Delta\delta_1 + \Delta\delta_4$, and $\Delta\delta_j$ as $\sum_{x=1}^{3} \Delta\delta_x$. Let $L_k$ denote the set of buffers in the clock tree path from the clock source to the clock input of any block $k$. Thus the change of delay of the clock input, $\Delta\delta_k$, can be expressed as a summation of delay changes of the buffers in the set $L_k$, and equation (6) can be rewritten as:

$$C_1 + \sum_{m \in Lj} \Delta\delta_m \le \sum_{n \in Li} \Delta\delta_n + \Delta D_{ij} \le C_2 + \sum_{m \in Lj} \Delta\delta_m \qquad (7)$$

If for instance $L_i = L_j$ (as shown in figure 6(b)), equation (6) and (7) reduces to:

$$C_1 \le \Delta D_{ij} \le C_2 \qquad (8)$$

In the absence of any active element on the interconnection between *i* and *j*, the timing constraint expressed in equation (6) vanishes, as the timing relation will always be satisfied even in the presence of p/g IR-drops.

***Observations***

(1) From theorem 1 it follows that the internal timing relations of the blocks need not be present in the formulation of the p/g mesh sizing.

(2) Timing constraints between all inputs and outputs in the fanin cone of a block *j* need not be checked transitively with respect to *j*. Since all input arrival times must satisfy the timing constraints at the input boundary of *j*, and all such blocks are synchronous and satisfy the property mentioned in observation (1), variables in the timing constraints are attributable to the immediate fanin interconnect elements and blocks.

(3) Simplification and elimination of timing constraints and variables external to the IP cores can be achieved as shown in equations (6) to (8).

## 4. Sizing Power/Ground Meshes

Similar to the traditional methods, our analysis is based on time-independent average current models for the p/g nodes. Thus, it is sufficient to model the p/g networks resistively. In reality however, the profiles of the currents flowing from and to the p/g node, will be time and input vector dependent. This will give rise to simultaneous switching noise (SSN), and hence will mandate the inductive, capacitive, and resistive modeling of the p/g networks. The linear programming formulation which we introduce in this section, will not be able to capture such SSN effects. Our present work is focussed on p/g mesh designing in the presence of SSN.

Given resistive p/g meshes (a power mesh is shown in figure 7; a ground mesh is similar) that drive a circuit of placed and routed synchronous computing blocks clocked by a given clock-network, our aim is to size the mesh for minimum area while satisfying the timing, electromigration, IR-drop, and design rule constraints. Any given segment *i* has a length $l_i$ and a width $w_i$. Whereas $l_i$ is fixed, $w_i$ is a variable in our formulation. Each clocked computing block is an IP core that draws a fixed amount of average current. All computing blocks, clock-network buffers, and active elements on interconnects that are placed inside a single square of the superimposed p/g meshes, draw the sum of their currents from a single node of the mesh as shown in figure 7. We assume that all timing relations are satisfied for perfect p/g node potentials. These timing relations exist both inside each computing block, and in the network of connected blocks for the placed and routed circuit with the given clock tree synthesized to achieve the desired frequency of operation.

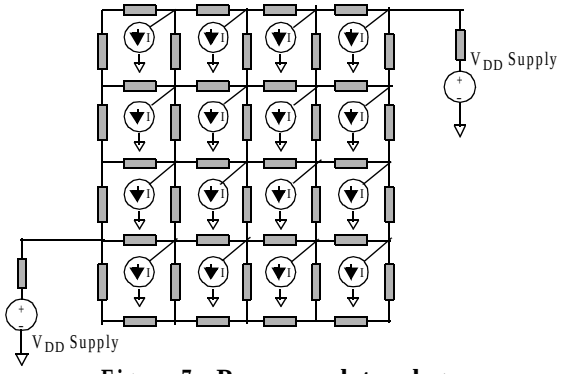



**Figure 7: Power mesh topology**

Besides the timing constraints as spelled out in section 3, the other constraints used in the existing methods for sizing p/g meshes are:

- Internal Timing Constraints

These are the timing constraints that need to be satisfied inside the synchronous blocks in the presence of p/g noise. As stated in theorem 1, these constraints can be equivalently expressed as a potential drop constraint of the power node $\Delta V_n$ of the block. For any block *k* inside a square in the mesh, let $V_k$ be the maximum allowable change of node potential in order to maintain internal timing constraints (theorem 1). Then the upper limit on the allowable change of the node potential ($V_{up}$) to maintain timing closure in the presence of p/g IR-drops is given by $V_{up}$ = minimum ($\forall_k V_k$), over all blocks in the square. Thus $V_{up}$ is different for different nodes in the power network, and the allowable drop of potential for each node ($\Delta V_n$) has to be less than the corresponding $V_{up}$: $\Delta V_n \le V_{up}$. Similar arguments hold true for the ground network.

- Minimum Width Constraints

In order to satisfy technological constraints, the width of any segment *i* of the p/g mesh is limited to some minimum width ($w_{i,min}$) according to the metal layer in which the segment lies: $w_i \ge w_{i,min}$

- Electro-Migration Constraints

The upper bound on the current ($I_i$) that can pass through a p/g mesh segment *i*, in such a way that the metal wire does not physically deteriorate, is given by: $\frac{|I_i|}{\sigma w_i} \le J_{max}$ . $J_{max}$ denotes the maximum allowable current density for the given technology, and $\sigma$ is the thickness of the segment.

- Maximum IR-drop Constraints

These constraints are required to ensure that the delays of active devices are linearly sensitive to IR-drops in their

supply nodes. Thus, the IR-drop of a power node *n* will be bounded by $\Delta V_n \leq V_{max}$, where $V_{max}$ is the upper bound of IR-drop that can be tolerated in a circuit. Similar relations hold for the ground nodes.

- Kirchhoff's Current Law

We assume that we have the flexibility of sizing each mesh segment independently. Let $S_n$ denote the set of mesh segments incident to any node *n*. If $I_k$ denotes the current flowing into (negative) and out of (positive) the node through any element *k* of $S_n$, then Kirchhoff's Current Law states that: $\sum_{k \in Sn} \vec{I_k} = 0$

The goal is to minimize the total area of the p/g meshes, which is given by: $\sum_{i \in all-segments} l_i w_i$ .

### 4.1 Sequence of Linear Programs Solution

Sizing a p/g mesh even under the set of linear constraints that we have, has been shown to be a non-linear programming problem when $w_i$ is expressed in terms of $l_i$, $I_i$, and the potential difference across a mesh segment *i*. In this paper we use the approach of [4],[7], wherein both the nodal voltages and branch currents are selected as variables in a 2-step procedure. In the first step node potentials are considered variables with fixed segment currents obtained from an initial solution of the given p/g mesh. In this case all constraints are linear, but the cost function is non-linear. We use the strategy adopted in [7] to linearize this objective function by taking a Taylor's expansion of the function around an initial feasible mesh solution, retaining only the constant and linear terms. The linearized function can be treated as an objective function provided that its monotonicity implies monotonicity of the original cost function.

In the second step the segment currents are variables and the node potentials are assumed fixed at the solutions found in the first step. This results in a linear program formulation. These two steps are repeated alternately with the initial conditions of any step being the final solution of the previous step, till the improvement in the cost function is below a certain preset threshold (the termination criterion). This yields the final solution.

## 5. Experiments

Our benchmarks are networks of interconnected IP cores, implementing MCNC and datapath circuits. These circuits were optimized from their *blif* representations using *sis*, and mapped to a pre-characterized library, which was generated by a commercial tool. All components of the library are input/output latched, and their load dependent delays and average currents are known. Besides, all the components operate at an internal frequency of 500MHz in 0.25µm technology with known input and clock slew rate requirements. A commercial placer and router were used to place and route the circuits. The interconnect parasitics are thereafter extracted, and timing is run. Each such IP core or computing block has an associated maximum allowable change of p/g potential value that can be tolerated for maintaining internal timing-closure in presence of p/g IR-drops. Our experimental results show that limiting the IR-drop to 10% the ideal supply voltage for any p/g node, is sufficient to satisfy the previous condition. For each circuit, a clock network, with allowable clock skews, is then synthesized to operate at 500MHz, while satisfying the slew rates requirements at the sinks. Our algorithm then sizes the mesh segments of the given power/ground grids with known topologies. The clock period remains unaffected during the optimization, and is treated as a constraint.

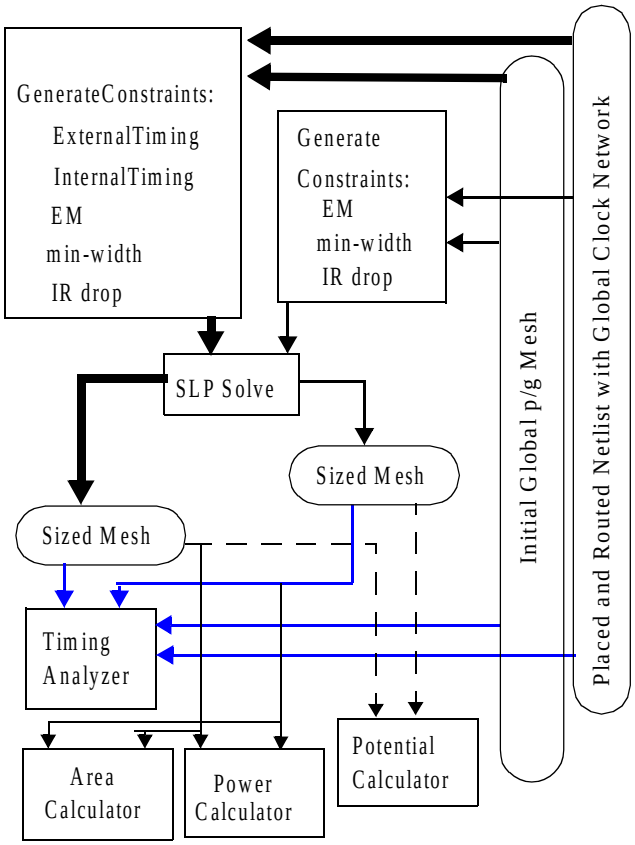



**Figure 8: Experimental flow**

Figure 8 shows our experimental flow starting with a given netlist of placed and routed computing blocks, the global clock-network and the initial global p/g meshes. The mesh sizing problem is then solved using the traditional method and our method (with the timing constraints). The resulting meshes obtained using both the methods are then

compared for timing violations, areas, node potential changes and circuit power dissipations.

## 6. Results

In figure 9 we show the percentage area improvements of our method compared to the efficient Sequence of Linear Programming method (SLP) [7]. We compare three different minimum power node potentials of 2.475V, 2.375V and 2.250V. The ideal supply level is 2.5V in the 0.25µm technology. All ground potentials are assumed ideal, but similar trends are observed if both the power and ground node potentials are considered to be non-ideal. Eight different netlists of IP cores are chosen as benchmarks. The area of the p/g mesh of a netlist is calculated by summing up the areas of the mesh segments. Our method improves the p/g mesh areas on an average by 29.52% compared to those of the SLP meshes when the minimum allowable power node potential is 2.475V. This improvement decreases to 24.36% and 13.85% on average, when the minimum power node potentials are restricted to 2.375V and 2.250V respectively. Allowing more IR-drops in the SLP method leads to thinner and more resistive wires in the meshes, which then occupy smaller areas.

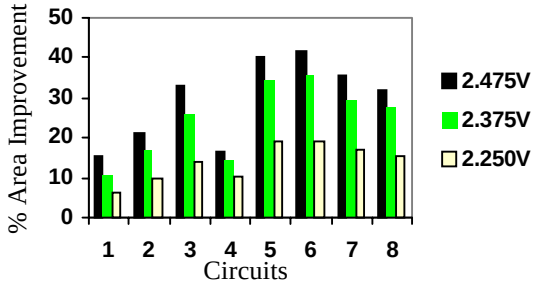



**Figure 9: Area improvement comparisons**

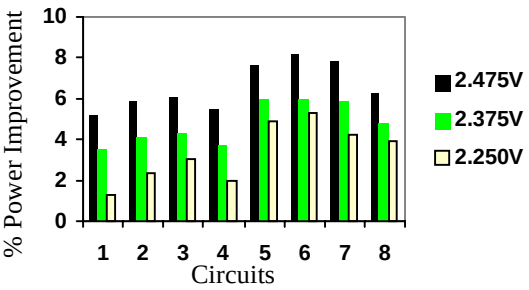



**Figure 10: Power improvement comparisons**

Figure 10 shows the power dissipation comparisons for the same set of benchmarks under the same conditions. The power dissipation of a netlist is found by adding the dissipations in the p/g mesh segments, with those of the individual logic or clocking elements. The power dissipation of a logic block or a clock buffer is found by multiplying the supply potential across it, with its average current. As the minimum power node potential decreases from 2.475V to 2.375V to 2.250V, the average power improvement decreases from 6.56% to 4.80% to 3.37% respectively. With decreasing power potentials, the power dissipations of circuit elements with fixed average currents decrease. The power advantage of our method decreases compared to the SLP method if more IR-drops are allowed in the latter.

Figure 11 shows the number of timing violations that the SLP formulation fails to remove. On average, this represents 1.73% of the total number of paths in the circuits. Since timing constraints are integral to our formulation, there will be no timing violations for the p/g meshes sized by our method. As we reduce the minimum allowable power node potential from 2.475V to 2.375V to 2.250V, the number of timing violations left unsolved by the SLP formulation increases on average, from 16.75 to 43.13 to 83 respectively, even though the mesh areas and power dissipations improve. This is the penalty paid by the traditional methods.

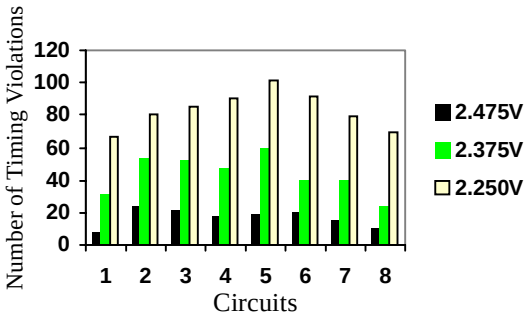



**Figure 11: Timing violations of the SLP method**

Note that our aim in this work is not just to achieve area and power dissipation improvements for the p/g meshes and the corresponding circuits. We are more interested in designing p/g meshes to achieve timing closure in the circuits, and the area and power improvements are useful incidental achievements. Hence, even though the area and power improvements decrease with lower potentials at the die supply pads, our analysis of the problem and its formulation remain very relevant.

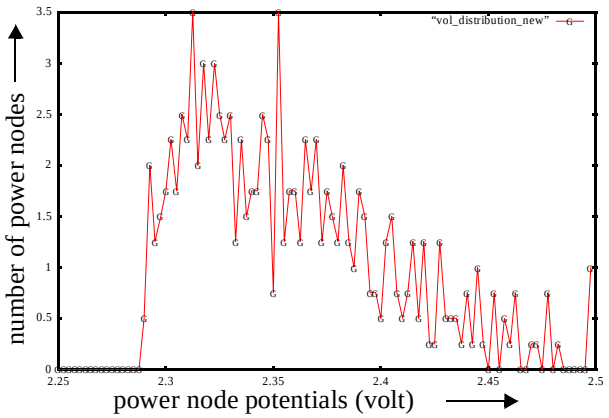



**Figure 12: Potential distribution obtained by our method**

In figure 12 we show the potential distribution of the power mesh nodes of a typical benchmark that has been sized using our method. The maximum IR-drop in the p/g meshes was constrained to be within 10% of ideal values. Different supply node potentials are shown on the x-axis, and the y-axis represents the node frequencies as percentage values of the total number of nodes in the mesh. A point on the plot corresponds to the percentage of supply nodes having a certain potential, as indicated by the x-axis value. The average node potential is deduced from the figure by adding the different node potentials, and dividing by the total number of power nodes in the mesh.

Figure 13 shows a similar distribution for the circuit as found using the SLP method with a minimum allowable node potential of 2.375V. In our case the average value of supply node potentials is lower than that of the SLP method because for the same number of supply nodes, the distribution in figure 12 is wider than the one in figure 13 (SLP method). This intuitively accounts for the lower power dissipation and mesh area achieved by our method.

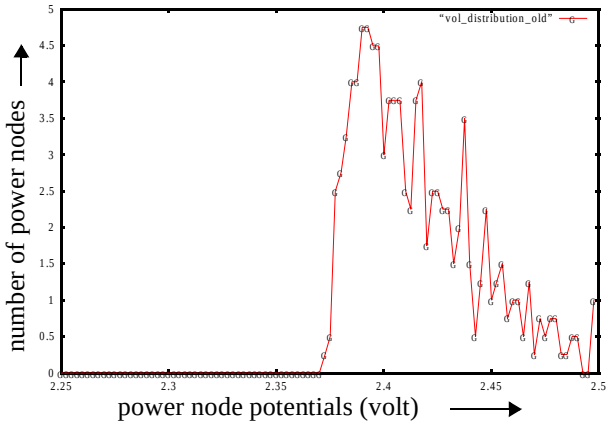



**Figure 13:**
**Potential distribution obtained by the SLP method**

All active components supplied from this network experience only the required potential drops across them to satisfy timing, and no more. This has the effect of reducing output peak-to-peak voltage swings for the active devices powered by the p/g meshes. Since the aging of transistors is proportional to the peak-to-peak voltage swings of their input transitions, our method slows down transistor aging, and leads to safer and more reliable circuits than those having their p/g networks designed by traditional methods.

## 7. Conclusions and Future Work

In this work we have established the importance of sizing power/ground networks while simultaneously considering the IR-drops induced by both the clocking and computing components in synchronous circuits. We have shown that traditional constraints are not enough to remove all IR-drop-induced timing violations, and on average, they may be leaving as many as 2% of the paths with timing failures. Experimental results demonstrate that our method with timing constraints achieves improvements of as much as 30% in area and 6.6% in power, compared to p/g meshes designed traditionally. Our solutions are obtained by limiting the maximum IR-drop at any p/g node to within 10% of the supply voltage, a commonly accepted bound for traditional methods.

As stated at the beginning of section 4, we are presently redesigning the p/g meshes to meet timing in the presence of simultaneous switching noise. We are further incorporating the flexibility of deciding the p/g mesh topologies in our formulation.

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