AnalogRouter: A New Approach of Current-Driven Routing for Analog Circuits*

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1. Introduction

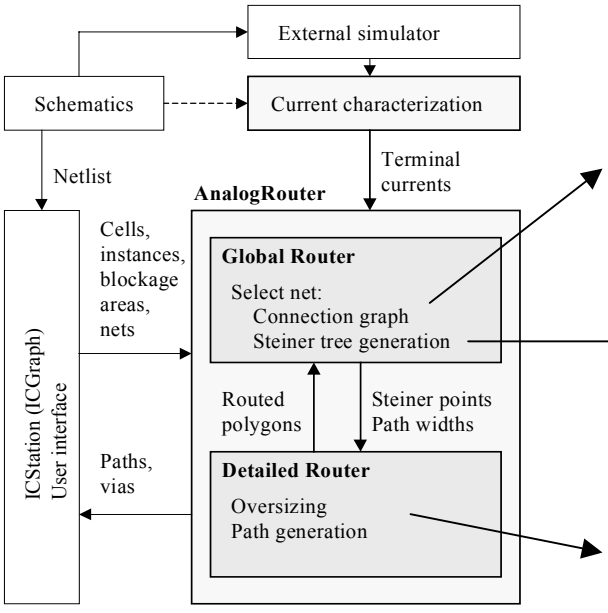
We present a new automatic routing tool, named AnalogRouter, specifically developed to address the problems of current densities and electromigration in routing of multi-terminal, non-planar signal nets in analog circuits.

The contributions of our work are:

- a new current characterization method based on current vectors attached to each terminal,
- current-driven Steiner tree generation which effectively determines all branch currents *prior to detailed routing*, and
- a run-time and memory efficient detailed routing strategy which addresses all features of current-driven routing for analog circuits, particularly varying wire widths.

2. Current-Driven Routing: Design Flow

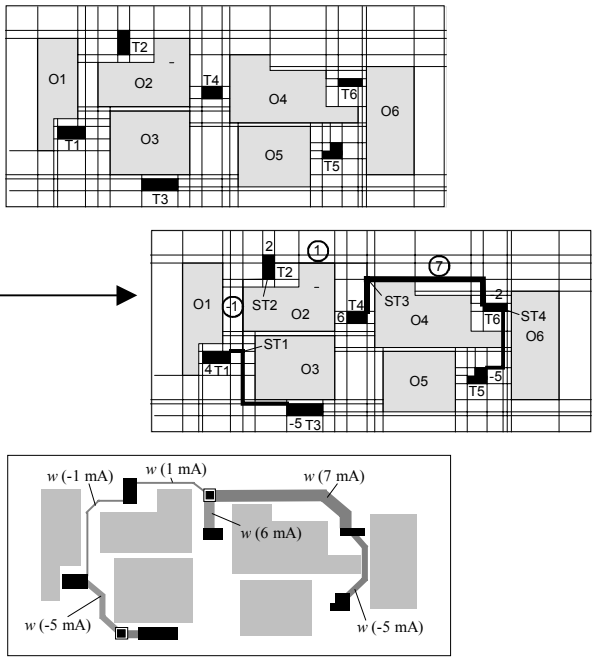
During current characterization, sets of "worst case" currents attached to each terminal are obtained. These values are transferred to the AnalogRouter either as part of the schematic netlist or as an ASCII file.



The AnalogRouter has been integrated into Mentor Graphic's ICStation environment which reads the netlist from the schematic tool. After an initial cell placement is generated, the main layout components (cells, instances, blockage areas and nets) are forwarded to the AnalogRouter.

During global routing, the nets are sorted in a "priority list" and a connection graph for the next net to be routed is generated. A Steiner tree is then established which represents both a valid topological route and a current-correct design of this net. The resulting Steiner points and the calculated path widths (derived from the path currents of the Steiner tree) are transferred to the detailed router. Here all previously established layout elements are oversized in accordance with the wire width of the interconnection to be routed next. Afterwards, a point-to-point (Steiner point or terminal point) path generation is performed. The routing path, which has been initially generated with a "default" width, is then widened to the current-correct size. (No further layout modifications are needed due to prior oversizing.)

The routed polygons of the net are returned to the global router in order to be considered in subsequent Steiner tree generations. Finally, all generated paths and vias are transferred to the main layout tool (ICStation).



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