On Automatic Analysis of Geometrically Proximate Nets in VLSI Layout

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Abstract

We address the problem of automatic analysis of geometrically proximate nets in VLSI layout by presenting a framework (named FASCL) which supports pairwise analysis of nets based on a geometric kernel. The exact form of the analysis function can be specified to the kernel, which assumes a coupling function based on pairwise interaction between geometrically proximate nets. The user can also attach these functions to conditions and FASCL will automatically apply the function to all pairs of nets which satisfy a condition. Our method runs with sub-quadratic time complexity, $O(N^{1+k})$, where N is the number of nets and we have proved that $k < 1$. We have successfully used the program to analyze circuits for bridging faults, coupling capacitance extraction, crosstalk analysis, signal integrity analysis and delay fault testing.

1 Introduction

With the rapid increase in design complexity and the simultaneous decrease in feature size, interconnect analysis has become an important task in computer aided verification of VLSI circuits. All reported formulations for interconnect analysis use some coupling analysis function on nets to form a crosstalk risk graph [4] or state the need for analyzing *neighbouring* pairs of nets with detailed techniques [1]. Since not all pairs of nets need to be analyzed to the same level of accuracy and because the parameters for analysis of nets change constantly, a fast and configurable geometric kernel needs to be developed which can *apply* specific analysis techniques to a set of nets which are close to each other. We refer to such a pair as geometrically proximate.

2 FASCL: The Proposed Approach

FASCL is an acronym for FASt calculation of Coupling functions in VLSI Layout. FASCL uses a scan-line based algorithm and has been implemented in Common Lisp. Previous scan-line based extraction techniques have been discussed in [2]. The input to FASCL is a Cadence DEF file, which contains information about routing geometry for each net. A default rule set based on coupling length and substrate capacitance has been built. Since the program itself is written in Lisp, it is very easy to add new rules based on APIs provided by the program. The APIs support query information on parameters like metal track number, orthogonal distance, coupling length, absolute length of interconnect and number of vias.

3 Experimental Results

FASCL was used to selectively analyze a subset of nets for bridge faults [3], with the condition that all pairs of segments, which are coupled for more than 50 units (as read in from the DEF file) and are on the same metal layer, should be analyzed (see Table 1 for computation time). The condition setting for the mode *BRIDGEFAULT* was :

```
COUPLEN=set_condition(*BRIDGEFAULT*)
begin
   ((layer_diff = 0) and (coup_len > 50))
end
```

Table 1. Computation Time for FASCL

Design	# Segments	Time (min)	Memory (MB)
D1	78681	0:04	20
D2	58769	0:14	20
D3	99217	0:30	53
D4	300486	0:46	118

Future work will concentrate on providing support for orthogonal coupling, non-Manhattan geometries and a GUI.

References

[1] A. Devgan, “Efficient Coupled Noise Estimation for On-Chip Interconnects”, in *Proc. ICCAD*, 1997, pp. 147–153.

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[4] A. Vittal and M. Marek-Sadowska, “Crosstalk Reduction for VLSI”, *IEEE Tran. CAD*, March 1997, vol. 16, pp. 290–298.