CMOS Sizing Rule for High Performance Long Interconnects

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Abstract

During the past fifteen years, the role of interconnects has turned to be the determining factor of the overall performance of VLSI circuits. In this work, the Authors present a new transistor sizing rule for long interconnect buffers. It is shown how transmission line properties of long interconnects alter the behaviour of the CMOS buffer, forcing transistors to work mainly in linear mode rather than in saturation as is usually assumed. This unusual condition leads to strong mismatching between predicted and actual driver output impedance if conventional sizing rules are used. The proposed sizing rule allows true line matching to be achieved, thus either minimizing delay or preserving signal integrity.

I. CMOS buffer sizing.

When long interconnect must be driven, buffer transistors are sized so that the on-resistance of the driver (R_{ch}) is equal to the characteristic impedance of the line (Z_0). This methodology allows one either to avoid multiple signal trips to switch the receiver, or signal over/undershoot, thus reducing delay and preserving signal integrity and device reliability. To achieve impedance matching, the channel width W_{ch} of transistors is then fixed assuming that during a low-high (high-low) transition, the Pmos (Nmos) is mainly in saturation.

Actually, if interconnect exhibit transmission line behaviour, during the switching transient it can be assumed the load seen by the switching gates to be a resistor of value Z_0. This implies that during the first phase of a $0 \rightarrow V_{dd}$ transition, the voltage at the output of the CMOS buffer, V_{near} is given by

$$\frac{V_{dd}}{(R_{ch} + Z_0)} Z_0 \quad (1).$$

If line is matched, by eqn.2, even though the input signal V_{in} to the gate reaches its steady value, output voltages remains constant and equal to $Vdd/2$ for twice the propagation time along the line, i.e. until the back-travelling wave reaches the source, as depicted in fig.1. It is easily verified that in these conditions, unusual for previous CMOS technologies, as soon as input voltage goes below $V_{dd}/2 + V_T$, the PMOS transistor operates in the linear region (obviously a similar condition holds for the NMOS during a $V_{dd} \rightarrow 0$ transition as well).

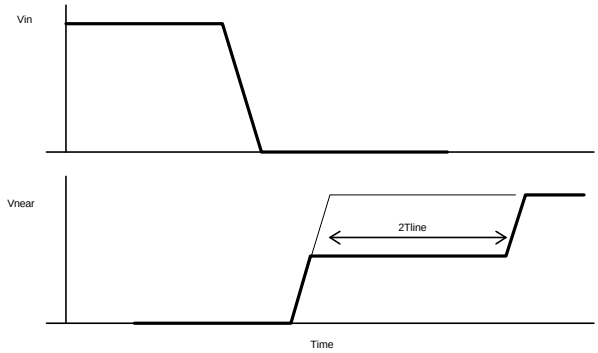

Figure 1. Input and corresponding output waveforms of the buffer.

Therefore, the more propagation time along interconnect is greater than transition time of the buffer output signal, the more transistor linear operation prevails over saturation. This strongly affects the on-resistance of the device and it appears evident that if propagation time becomes relevant with respect to signal transistion time, conventional sizing based on eqn. 1 leads to significantly undersized transistors. In the work the Authors present a developed sizing rule for true line-matching. HSPICE simulations have been carried out for two different CMOS technologies and they confirm that the linear region better describes the switching operation of transistors and the effectiveness of the proposed sizing rule for driver/line matching.