# Susceptibility of Analog Cells to Substrate Interference

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## Abstract

*This paper deals with the susceptibility of smart power integrated circuits to substrate interference. In particular, propagation of RF interference through substrate and its effects on analog cells are investigated. A new method, developed to identify a parasitic substrate-coupling network in VLSI devices, has been customized for a smart power technology process. The layout view of a specific circuit is elaborated in order to extract a netlist composed of circuits in the die surface and the substrate parasitic network. Predictions are obtained by executing time-domain simulations. A simple test circuit composed of a power transistor and an OTA is considered. Investigations are carried out for various layout of the same test circuit and the effectiveness of shielding substrate contacts is evaluated.*

## 1. Introduction

Nowadays, smart power technology processes make it possible the design and realization of complex ICs composed of analog, digital and power blocks. In many cases a complete electronic module is collapsed into an IC. In these devices, RF interference reach active and passive integrated components by metal interconnection routed on the silicon surface, or through parasitic paths. Since 50-70 % of a smart power device area consists of power transistors, an effective capacitive coupling with silicon substrate is realized and RF interference, collected by cables, is injected directly into the substrate through the power-transistors isolation diodes. Unfortunately, silicon substrate does not behave as a common ground plane and a part of the interference injected through power transistors reaches other components realized in the same die. RF interferences collected by the substrate drive non-linear phenomena in active components and failures in analog circuit operations occur.

## 2. Substrate Coupling Analysis

In this work the algorithm developed by Gharpurey et. al. [1] has been customized for a smart-power technology process [2]. Each active and passive device has been characterized in terms of substrate capacitive coupling, and parasitic elements have been included in each device model. The network composed of surface circuits and substrate parasitic interconnections is obtained by elaborating the circuit layout view and the substrate doping profile descriptions. In particular, the layout view (including power devices) is elaborated and an extracted view is obtained. On the basis of such a description the substrate parasitic network is extracted and linked with the network of surface components. Hence, a SPICE-like netlist is obtained. Time-domain simulations of the extracted netlist allows predicting the non-linear effects induced in the die surface circuits by RF interference coupled via substrate.

In this work the layout of several analog cells like OTAs, bandgap and VCOs circuits have been designed. Each layout has been elaborated by the procedure described as above. Time-domain simulations of each network extracted from the layout view (which include substrate parasitic network) have been performed and effects of substrate interference have been evaluated.

## 3. Conclusions

This paper presents result of investigation concerning the immunity of analog cells to substrate RF interference. Investigations have been carried out for several analog cells and the effectiveness of substrate contacts has been evaluated. Simulation results have shown that the susceptibility reduction related with substrate-shielding structure is negligible if compared with effects on the circuits quiescent operating variations due to RF sources amplitudes and impedance modifications.

## References

[1] R. Gharpurey, R. G. Meyer, “Modeling and Analysis of Substrate Coupling in Integrated Circuits”, *IEEE J. of Solid-state Circuits*,vol. 31, NO 3, pp. 344-352, 1996.

[2] Multipower BCD60-III, Design Manual, Rev. C.0, STMicroelectronics, Aug. 1997.