An Improved Hierarchical Classification Algorithm for Structural Analysis of Integrated Circuits

Markus Olbrich
University of Hanover
olbrich@ims.uni-hannover.de

Achim Rein
Infineon Technologies AG
achim.rein@infineon.com

Erich Barke
University of Hanover
barke@ims.uni-hannover.de

Abstract

A new and efficient combination of signal tracing and block recognition techniques for circuit analysis is proposed. It utilizes the benefits of both approaches to solve problems such as signal flow or gate recognition. The analysis process is easily controlled by a user definable rule set where ports, nets and blocks are attributed with types. After structural investigation a hierarchical netlist is produced providing block information as subcircuits. As an important feature, the algorithm allows the handling of optional ports as well. Thus, this flexible approach is applicable to various circuit types and works on several abstraction levels.

Classification Algorithm

At several stages in a design flow the current status of a design has to be analyzed. This often requires a transfer to a higher abstraction level. In contrast to previous methods ([1], [2], [3]), our pattern based classification approach extends a combination of block recognition with a new type assignment concept [4].

Types are used for object classification. There are types for ports, nets and elements. Each of these objects can have an arbitrary set of types simultaneously. Each **block rule** contains a pattern of a circuit part to recognize (block) and a set of **conclusions**. They determine type assignments when a match is found.

A user defined **rule set** controls the analysis process. It is composed of both type declarations and block rules. When a block rule matches, two actions are performed: First, appropriate conclusions are assigned and second, a subcircuit is inserted. This causes other blocks to meet the matching requirements as well. As an advantage of this procedure, an inserted subcircuit can again be reused as a part of a matching block. Thereby, the circuit representation is restructured by inserting subcircuits and objects are classified by assigning types.

Fig. 1 shows an example. Given an appropriate rule set, the analysis of the circuit a) will result in b). The resistor path is successively grouped, the inverter is recognized and signal direction is traced. The classification algorithm is able to work on any hierarchical netlist. We used the algorithm for the analysis of analog circuits as well.

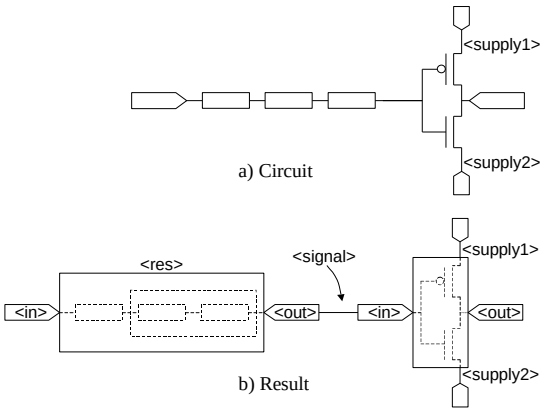

Fig. 1: Example

As extended features for block recognition we allow the treatment of optional and multiple ports. In some cases it is desired to put adjacent elements together like the resistor chain in the example above. Special adjacency rules are defined for this purpose.

Since run time is an important issue we found that the revisiting of rules leads to many unsuccessful matching tests. We developed an automatic revisit ordering with less matching tests that leaves the result invariant.

Run-time depends on the rule set and the circuit to be analyzed. With some preconditions the number of subgraph isomorphism tests is limited to $O(n^2)$. Examples confirm this assumption.

References

[1] Kubo, N.; Shirakawa, I.; Ozaki, H.: *A Fast Algorithm for Testing Graph Isomorhpism*. ISCAS, pp. 641-644, 1979.

[2] Ohlrich, M.; Ebeling, C.; Ginting, E.; Sather, L.: *SubGemini: Identifying SubCircuits using a Fast Subgraph Isomorphism Algorithm*. DAC, pp. 31-37, 1993.

[3] Singh, K. J.; Subrahmanyam, P. A.: *Extracting RTL Models from Transistor Netlists*. ICCAD, pp. 11-17, 1995.

[4] Olbrich, M.; Rein, A.; Barke, E.: *Ein neuer hierarchischer Klassifizierungsalgorithmus zur strukturellen Analyse integrierter Schaltungen*. Analog 99, 1999.

We thank Infineon Technologies AG, Department MP PTS. This work was supported by the German Bundesministerium für Bildung und Forschung under contract 01 M 3034. The authors are responsible for the contents of this publication.