Exact Fault Simulation for Systems on Silicon that Protects Each Core's Intellectual Property (IP)

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Abstract

*We present a fault simulation approach for multi-core systems on silicon (SOC) (a) that provides **exact** fault coverage for the entire SOC, (b) does so without revealing any intellectual property (IP) of core vendors, and (c) whose run time is comparable to that required by the existing approaches that require all IP to be revealed. This fault simulator assumes a full scan SOC design and is first in a suite of simulation, test generation, and DFT tools that are currently under development. The proposed approach allows flexibility in selection of a test methodology for SOC, reduces test application cost and area and performance overheads, and allows more comprehensive testing.*

1 Introduction

We have developed a paradigm for development of SOC specific tests, which ensures IP protection of each of its constituent cores by processing each core's netlist on a secure computer, approved by the core's vendor. It is envisioned that instead of providing a test set or netlist of a core, the core's vendor allows the SOC designer to make **query/request** to their CAD procedures. The core's proprietary information, such as its layout and netlist are encapsulated in core-level procedures which are executed on secure computers. Furthermore, SOC-level procedures are allowed to make only those queries and requests that reveal non-proprietary information about the core. Finally, procedures themselves are envisioned as guaranteed (say by being developed by a reputed, independent CAD vendor) to provide only non-proprietary information, such as response to specific vectors, to the SOC-level procedures. Note that core vendors already release such information since they provide models for simulation and verification. Under this paradigm we have implemented a gate-level SOC fault simulator for stuck-at-fault model.

2 Query/request fault simulator

We have proven that completely accurate fault simulation can be performed by querying each core for non-proprietary information, namely (a) response at core outputs for a given combination of values at its inputs, and (b) the response at outputs for a faulty version, if the target fault is located within the core.

We have implemented some advanced techniques for efficient fault simulation in query/request paradigm. Techniques implemented are parallel pattern serial fault simulation, reconvergent stem fault simulation within the stem region [MR 90], critical path tracing for fan out free regions, etc. Some of the key procedures implemented at the SOC level as well as at the core level perform following tasks. (a) Identifying reconvergent stems adapted from [MR 90]: Stems are assigned unique identification numbers across the system to protect core stem information. (b) Event driven logic simulation in forward levelized order. (c) Critical path tracing for the fan out regions in forward levelized order: This processing determines which faults within the fanin cone get propagated to the stem due to the current packet of test vectors. (d) Event driven fault simulation of the reconvergent stem faults in forward levelized order. (e) Determination of criticality of the stems with respect to system primary outputs in reverse levelized order: For the non-reconvergent stems criticality is determined from the criticality of the fanout stems and for reconvegent stems criticality is determined from the criticality of the exit lines. Fault dropping and the reduction of the circuit area with no faults in the fanin cone is also performed. Steps (b) to (e) are repeated for each packet of test vectors. Each type of processing is performed in event driven breadth-first manner to reduce the information exchange between SOC and core level procedures. Details of the algorithms can be found in [QG 00b].

3 Conclusion

We have demonstrated that the proposed simulator provides complete accuracy at 30-40% overhead in fault simulation time complexity. Only intellectual property that is revealed in this process is input/output dependency. We have demonstrated elsewhere how the ability to generate SOC specific tests can significantly reduce DFT overheads as well as test application time [QG 00a]. This paradigm has been extended for ATPG and fault simulation for both sequential and combinational circuits.

Reference

[MR 90] F. Maamari and J. Rajski, "A Method of Fault Simulation Based on Stem Regions," in *IEEE Transactions on Computer-Aided Design*, Vol. 9, No. 2, pages 212-220, February 1990.

[QG 00a] Md. Saffat Quasem and Sandeep K. Gupta, "Test Information for Cores: Comparative Analysis and Recommendations," in *International Workshop of Testing Embedded Core-based System-chips 2000*.

[QG 00b] Md. Saffat Quasem and Sandeep K. Gupta, "An Exact Fault Simulation for Systems on Silicon that Protects Each Cores's Intellectual Property (IP)", *Technical Report CENG 00-06*, University of Southern California, LA, CA, 2000.