Towards a Better Understanding of Failure Modes and Test Requirements of ADCs

A. Lechner[1], A. Richardson[1] & B. Hermes[2],
[1] Faculty of Applied Sciences, Lancaster University, Lancaster, LA1 4YR, UK.
[2] Philips Semiconductors, Millbrook Industrial Estate, Southampton, SO15 ODJ, UK.

Abstract

It is now widely recognised that Built-In Self-Test (BIST) techniques and Design-for-Testability (DfT) will be mandatory to meet test and quality specifications in next generation mixed signal ICs [1]. For evaluating, verifying, and comparing testability improvements, a more detailed understanding of circuit specific failure modes is essential. This paper presents fault simulation results for a 6-bit ADC and identifies typical failure modes the converter is likely to exhibit and hence must be tested for.

1. The Target ADC Design

The converter under investigation, a 6-bit 330MS/s differential folding ADC, is implemented in a 0.3µm standard CMOS process. The layout occupies 0.1mm^2 of silicon and contains 1050 transistors. 75% of the silicon area is dedicated to analogue circuitry. The analogue section of the converter comprises a resistor ladder to generate the differential reference voltages, two amplifier arrays, a track & hold array, and a comparator array. The analogue circuitry has been fault simulated by the use of fault simulation models similarly to those presented in [2]. The layout extracted weighted fault list has been reduced from initially 4469 to 629 candidates, as identical faults affecting identical signal paths within the ADC only require analysis once.

2. ADC Fault Simulation

A transient simulation for a ramp input stimulus has been chosen to evaluate the ADC's failure modes. This also allowed computation of test coverage figures for the analogue front-end partial BIST structure presented in [3]. Apart from *offset* and *gain* values, minimum and maximum code width (*CW*), and integral non-linearity (*INL*) have been computed. Figure 1.a also illustrates fault coverages for a number of average current measurements at various voltage sources (*Meas.*), current consumption in power-down mode (*I(pwd)*), and the accumulated test coverage (*Accu.*). Only a small proportion of faults are detected by one test only (*unique* in Figure 1.a). Faults not causing failure in any of theses tests were categorised and are subject to further analyses.

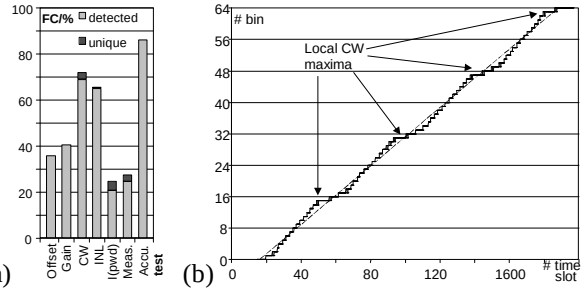

Figure 1: ADC failures and failure modes

3. ADC Failure Modes

Figure 1.b illustrates an example of a likely failure effect, for example, due to a short between resistors or through gate oxide. Generally, a significant proportion of faults contribute to failure modes that degrade performance specifications. Also, analysing the test response allows some fault diagnosis, for example if upper or lower bits are affected or if the fault occurred before or after the folding operation. Another interesting result is that the robust ADC design can compensate for high ohmic shorts and parametric faults. These results support the use of defect-oriented test analysis procedures and associated fault simulation tools to derive optimised test plans and built-in test structures.

[1] SIA: 'International Technology Roadmap for Semiconductors, 1999 Edition', 1999
[2] A. Lechner, A. Richardson, B. Hermes & M. Ohletz: 'A design for testability study on a high performance automatic gain control circuit', VTS98, pp.376-385
[3] A. Lechner, J. Ferguson, A. Richardson & B. Hermes: 'A partial built-in self-test for a high performance automatic gain control circuit', DATE99, pp.232-238