TESTABILITY TRADE-OFFS FOR BIST RTL DATA PATHS: THE CASE FOR THREE DIMENSIONAL DESIGN SPACE

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Abstract

Power dissipation during test application is an emerging problem due to yield and reliability concerns. This paper focuses on BIST for RTL data paths and discusses testability trade-offs in terms of test application time, BIST area overhead and power dissipation.

It was reported in [4] that there is significantly higher switching activity during testing than during functional operation and hence higher power dissipation. The aim of this paper is to examine testability trade-offs for built-in self-testable (BIST) register-transfer level (RTL) data paths, and based on exhaustive experimental data to justify the need for a three dimensional testable design space which needs to be considered while exploring alternative solutions.

The experimental validation flow is employed for 32 point discrete cosine transform (DCT) data path with 60 registers, 9 multipliers, and 12 adders. The modules at RTL, used by the high-level synthesis system [2], and test registers are synthesized and technology mapped into AMS 0.35 micron technology [1]. The test length for adders and multipliers is considered $T_+ = T_u$, and respectively $T_* = 4 \times T_u$, where $T_u = 128$ for achieving 100% fault coverage for 8 bit data path modules. Figure 1 shows the three dimensional testable design space for 32 point DCT. Since plotting the entire solution space ($\approx 10^{23}$)is beyond the computational capabilities of the state of the art computing resources, the results have been obtained by randomly generating 33,500 BIST data paths which is a representative testable design space of the entire solution space. Unlike the case of exploring *only* test application time and BIST area overhead or *only* test application time and power dissipation, the exploration of the three dimensional design space accounts for *all* the three parameters: test application time, BIST area overhead, and power dissipation. The main advantage of exploring the three dimensional design space is that solutions equivalent in terms of BIST area overhead and test application time (power dissipation and test application time) with different values in power dissipation (BIST area overhead) are not ignored. Since, for the particular example of 32 point DCT, the size of the solution space is huge, techniques with low computational time need to be developed [3] in order to efficiently search the three dimensional design space. Further, it is anticipated that the three dimensional testable design space presented in this section is not valid only for BIST embedding methodology for RTL data paths, rather it can be extended to the much more general case of BIST for systems-on-a-chip (SOC).

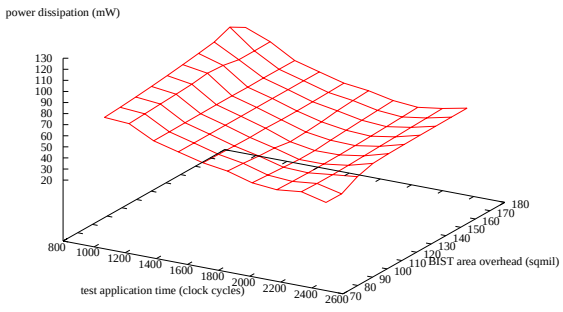

Figure 1. Testable design space.

References

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