Retargeting of Mixed-Signal Blocks for SoCs

R. Castro-López, F. V. Fernández, M. Delgado-Restituto and A. Rodríguez-Vázquez
Instituto de Microelectrónica de Sevilla, Centro Nacional de Microelectrónica, Sevilla, SPAIN
Phone: +34 955056666, FAX: +34 955056686

Abstract

This paper introduces a very efficient methodology for retargetability of embedded mixed-signal blocks for SoCs. The key parts of this methodology are: parameterised layout templates at different hierarchical levels, accurate behavioral modeling of mixed-signal blocks and appropriate mechanisms to tuning sized circuits to new sets of specs.

1. Introduction

As chip complexity explodes and compressed product development cycles relentlessly scale time-to-market pressures, designers must accomplish more ambitious objectives in less time. For an increasing number of designers, the secret to quickly building highly integrated systems on a chip (SoCs) in a shrinking development cycle lies in the extensive reuse of silicon-proven megafunctions or blocks.

In this context, new design paradigms have to be found which provide a significant increase of the design productivity. This is particularly important in the area of analog and mixed analog-digital designs where the levels of design automation are well behind those achieved in the digital domain. Retargetability for reuse can significantly increase the design productivity of mixed-signal designers, especially having in mind the need to achieve very short cycles of technology migration.

This paper introduces a retargeting methodology with special emphasis on mixed-signal designs. The basic flow of this methodology is presented in Section 2, while Sections 3 to 5 discuss its basic components: parameterized reusable layouts, block behavioral models and hierarchical tuning strategy.

2. Retargeting methodology

The design flow to carry out the retargeting of an existing design to new specifications and/or a different technology is illustrated in Fig. 1. First, the set of specifications are validated by checking that they are within the range of retargetability of the blocks. The design is carried-out only if the specifications are validated, meaning that the new set of specifications falls within the range of the retargetability of the block. In principle, it is possible to define the range of retargetability so that the occurrence of unfinished designs is minimal. Nevertheless, by carrying out a tentative retargeting of a block based on assumptions of the validity of the specifications and by progressing through the different levels of the design, it is always possible to determine whether the design, indeed, cannot be concluded.

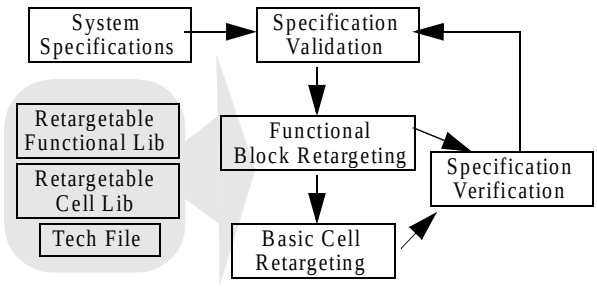

Figure 1. Flow diagram of the retargetable design environment.

The retargeting process proceeds hierarchically by tuning the existing designs to the new specifications. After tuning the functional building blocks, there is a process of tuning the component cells within each functional block. Tuning at any hierarchical level only affects the parts of the circuit components that need to be changed.

The tuning of each block at each hierarchical level is performed using the iterative mechanism illustrated in Fig. 2. In case the design is being migrated to a different technology the existing layout templates are updated taking into account the layout design rules of the new technology. Layout extraction yields updating of the component block models (transistor-level description at the cell level and behavioral models at all other hierarchical levels). Block behavior is obtained by simulation (electrical simulation for transistor-level descriptions and behavioral simulation for intermediate blocks). According to the simulation results size corrections are performed. This is the starting point in the retarteting flow in case that a new set of specifications must be met without a change in technology. For intermediate hierarchical levels, the outcomes of the size correction task are appropriate specifications for lower level blocks. At the cell level, size corrections directly provide suitable changes in device sizes. Application of changes to the layout templates allows to close the retargeting cycle.

Obviously, stopping mechanisms break this loop,

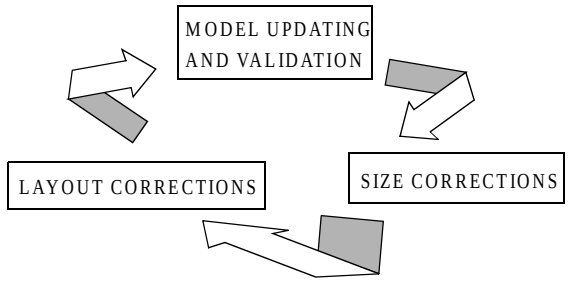

Figure 2. Retargeting cycle at each hierarchical level.

when either the specifications for the block at that hierarchical level have been achieved or it is impossible to arrive at an appropriate solution. In the latter case, backtracking mechanisms impose additional constraints on the retargeting process at upper hierarchical levels.

After the tuning of all the functional building blocks and circuit components has been completed, it is necessary to verify the correctness of the new performance characteristics and then proceed to the final processing and verifications.

The operation of the retargeting methodology proposed here will be demonstrated in this tutorial through the design of the mixed-signal blocks of the I/Q DAC transmit interface in Fig. 3. The original design for GSM specs in the AMS 0.35µm technology will be migrated to other technologies and a new set of specifications.

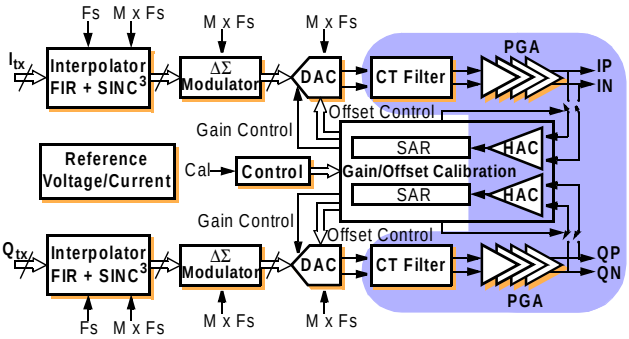

Figure 3. Block diagram of an IQ DAC.

3. Parameterised reusable layouts

Layout corrections have to be provided at the different hierarchical levels. The objective of reusability is not to obtain the optimum design, but to reduce the time-to-market of a design whose performance accomplishes the required specifications.

To this end, layout corrections are based on the tools, methods and languages available in the Cadence DFWII framework. The use of p-cell technology [1] makes an intensive use of parametrization, hierarchical cells, inheritance through hierarchical cells, and symmetries. The capability of p-cell technology to generate SKILL code, which can be externally modified enables a full technology portability of the generated layouts.

4. Behavioral models

The objective of behavioral modeling is to represent circuit functions using abstract mathematical models that are independent of circuit schematics or architectures. They enable the reduction of the simulation time of the system, a very important feature in this context, since these behavioral models will be used in an iterative cycle of optimization and verification.

For digital circuits, behavioral modeling can be performed with high-level description languages such as VHDL or Verilog, but these languages are not appropriate for a right behavioral description of analog systems, since the analog characterization is composed not only of the function that the circuit has to perform, but also the second-order non-idealities intrinsic to analog operation. Therefore, a suitable *analog high-level description language* with enough resources to implement those second-order effects must be used to create correct behavioral models of analog circuits.

Efficiency/accuracy trade-off of behavioral models of analog blocks is parameterised. When tuning subblock specifications, efficient, less accurate models are prefered to enable a fast, wide exploration of the design space, whereas for validating block behavior accurate models must be used.

5. Size retargeting

Size retargeting, both at the cell level and the functional level, is performed using both deterministic and statistical optimization methods. Deterministic methods are much faster and in normal conditions should suffice for a retargeting process. Statistical methods, although more expensive in terms of computation time, become active in case that deterministic methods are not able to achieve the retargeting objectives.

A statistical optimization technique, inspired on simulated annealing methods, has been developed whose control parameters offer different trade-offs between speed and quality of the retargeting results.

A modular and flexible structure of the optimization core allows the incorporation of system-specific design rules and constraints, constraints from the existing layout templates for the different blocks, and evaluation procedures of the quality of the retargeted layout cells.

6. References

[1] “Virtuoso Parameterized Cells Reference Manual”, Product Version 4.4.1, February 1997, Cadence Design Systems, Inc.