A SKILL™-based Library for Retargetable Embedded Analog Cores

Xu Jingnan[1] João Vital[1,2] Nuno Horta[1]

[1] Instituto Superior Técnico
IST Centre for Microsystems
Av. Rovisco Pais, 1
1096 Lisboa Codex – PORTUGAL

[2] ChipIdea - Microelectrónica, S.A.
TagusPark, Ed. Inovação IV, Sala 733
2780-920 Porto Salvo – PORTUGAL

Abstract

This paper describes the automatic generation and re-usability of physical layouts of analog and mixed-signal blocks based on high-functionality pCells that are fully independent of technologies. The high-functionality pCell library presently contains over 42 pCells and is fully compliant with 7 different sets of technology design rules from 5 different foundries. Practical examples employed in industrial projects are illustrated.

1. Introduction

In the past decades, efforts were dedicated to the development of layout automation methodologies for analog circuits. A tool, which can automatically generate full-custom layouts for analog circuits was presented in [1]. Various types of circuit compilers were also proposed for fixed circuit topologies, such as the Continuous-Time Filter compiler described in [2]. Besides these, basic transistor cell generators were also developed to increase the productivity of layout design [3]. More recently, a methodology to generate analog circuit stack was proposed, based on the analysis of the circuit algorithm and considering the matching problems in analog circuits [4].

Despite these significant research efforts, full deployment of analog CAD tools into professional environments is still very limited. This significantly limits the productivity that can be achieved by analog and mixed-signal design teams, especially when compared with the much higher levels of design automation typical of digital design environments.

The first generic method of layout re-use/retargeting presented here is based on layout parameterization fully independent of technology. The second method is based on retargeting an original template, and is currently limited to very simple operations.

2. Retargeting Methodology and Approaches

Several different steps can be identified in the process of retargeting an analog or mixed-signal block, be it either between different technologies or in the same technology but for different specifications. It is assumed here that the topology of the circuit remains fixed and, therefore, the whole procedure begins by redefining the sizing of the circuit to be compliant with new technology and/or specifications. Once this is achieved, the necessary layout modifications are implemented and the whole new database is re-simulated for final validation and eventual fine-tuning. The work presented in this paper is focused on the automation of the layout retargeting, and is a part of a Project for automation of the full retargeting process.

A true retargeting mechanism should have the possibility to perform only the necessary changes on an original layout database, without requiring any special preparation of this layout, and deliver the retargeted layout DRC and LVS error-free. However, it is not hard to understand that such ideal approach is extremely complex to implement. It must resort to component extraction capabilities and LVS mechanisms to identify what are the layout components to be modified, and then implement the changes with no disruption of connectivity.

While the techniques for such a beautiful approach are being developed, simpler alternative techniques can lead to relevant improvements on productivity. The most common solution is the development of module generators, which can be either template-based or performance driven. However, the concept of retargeting is more diffuse in these cases, since what happens is truly a complete automated redesign of the layout. The concept we used in this work is slightly different, because it is based on the hierarchical development of a library of parameterized layout cells (pCells) and auxiliary functions which are used to describe layouts from the very simple polygon layer shape up to large cells with high-level of complexity. The layout retargeting is implemented then by changing parameters according to different circuit sizing and by attaching different technology files to the pCells. A second method, described later on in this paper, performs a number of simple operations over an original database to make it compliant with new DRC rules.

3. Technology Independence

The key for technology independence is the correct definition of a minimum set of generic DRC parameters that allow the description of all layout constraints imposed by a large number of different technologies. A simple example of such parameters for the basic MOS device is shown in Fig. 1. Care must be taken on the definition of the basic devices to cover all the particularities specific to each foundry. This means that the logical constructions of the basic devices must be accompanied by a number of possible variants with generic layers, which can then be either mapped into dummy layers or into specific layers of the technology.

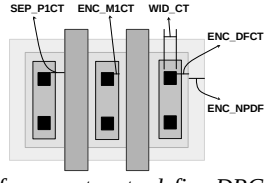

Fig. 1: Example of parameters to define DRC constraints.

4. Parameterized Cells and Functions

This work is fully developed within Cadence Design Framework (CDF) and uses SKILL language [5]. There are many useful functions within the CDF, which allow to access the database and to design pCells and graphical interfaces.

Two different libraries were built to support the envisaged layout retargeting methodology. The library of functions was developed to form a basis on the top of which the pCells were programmed. It deals with such basic problems as drawing polygon shapes according to the technology constraints, getting dimensions of a specified layout structure, identifying pins in a database, routing nets between pins, etc. The library of pCells contains the parameterized layouts hierarchically organized from the simplest MOS, resistor and capacitor devices and substrate/well bias geometries, to the more complex cells such as operational amplifiers, bias generation circuits, digital gates and complete DACs cells.

The development of the libraries and functions was based on the definition of a technology file that contains the parameters for DRC constraints of the technology, as explained in the previous section. This file is customized to support each specific technology, and is attached to the cell whenever this cell is to be ported to the considered technology. The high-functionality pCell library presently contains over 42 pCells and is fully compliant with 7 different sets of technology design rules from 5 different foundries.

5. Ultra pCells - Case Study

The demonstration vehicle of our project is a ultra pCell for a complete IQDAC core to be used on an interface for wireless applications. The current-steering DAC block diagram is represented in Fig. 2. Two different instantiations of the resulting pCell in different technologies are represented in Fig. 3. These results were obtained with the same pCell and the same parameters, but attaching a different technology file to the cell. There are 73 input parameters in the DAC core pCell, which can control the length and width of every transistor and can also change the width of some power supply lines, such as vdd, gnd and outputs, etc. In order to avoid unexpected errors, it is given the freedom to the user to move some cell blocks in *x* direction or *y* direction in order to accomodate large layout variations.

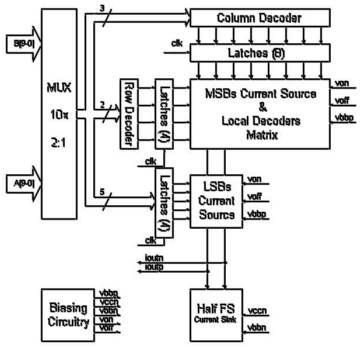

Fig. 2: Current-steering DAC block diagram.

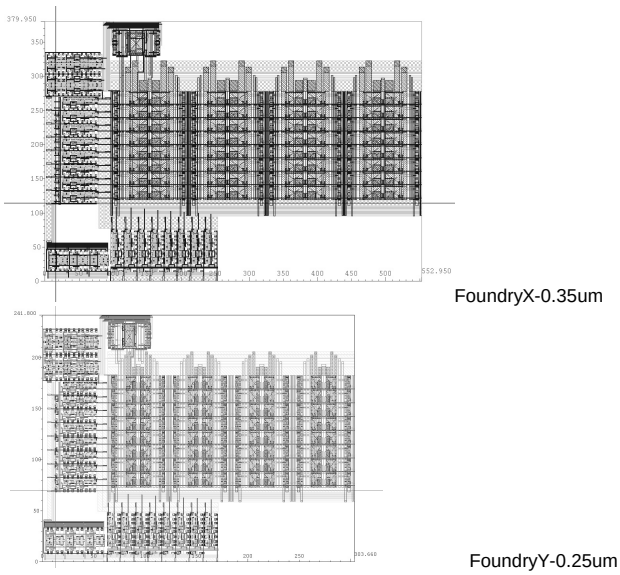

Fig. 3: Instantiation of the DAC pCell in different technologies.

6. Layout Direct Retargeting Tool

The principle behind the Layout Direct Retargeting Tool (LDRT) is to generate a new database that differs from the original in the following aspects dependent on the target technology: layer names; dimensions of contacts and vias; adjustment to a different grid-size; multiplication by a scaling factor. These simple operations are of great help when porting analog circuits between different technologies with similar electrical characteristics, and in non-critical digital circuitry. The tool has been coded using SKILL and is fully integrated in CDF.

7. Conclusions

Two different methods for retargeting the layout of analog and mixed signal circuits are presented. This first is based on layout parameterization and covers a large range of circuit complexity levels. The second method processes an original database, which does not need to have an initial preparation, to create a new database compliant with a different set of DRC rules.

Acknowledgments

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