Analog/Mixed-Signal IP Modeling for Design Reuse

N. Martínez Madrid*, E. Peralías, A. Acosta, A. Rueda

Instituto de Microelectrónica de Sevilla (IMSE-CNM), University of Seville, Spain
**FZI Karlsruhe, Haid-und-Neu-Str. 10-14, 76131 Karlsruhe, Germany*
martinez@fzi.de peralias@imse.cnm.es

Abstract

The application of design reuse to analog and mixed-signal components for System-on-Chip (SoC) is an emerging and revolutionary field. This paper presents a methodological approach to this area illustrated with a mixed-signal case study.

1. Introduction

Analog and mixed-signal design has turned out to be a hot topic in the industry and academia since analog and mixed-signal devices need to become part of SoCs. Typically, these SoCs are programmable general-purpose systems integrating at least one processor or controller core with many functions of the end product. They also need to integrate real-world interfaces such as data converters, filters or phase-locked loops. The main requirements for these components are low cost and feature-set requirements, which will bring benefits from the design and allow their reusability in a broader family of products.

This SoC complex environment requires a drastic change of design methodology. In digital design, a major movement has been undertaken in the last years by introducing design reuse of Intellectual Property (IP) modules, thus forcing designers to use a top-down design methodology for which behavioral modeling at different levels of abstraction are needed. Although not yet comparable to the digital IP market, there are already many companies selling analog cores and associated services ([1]). However, due to the specific features of analog design, almost all analog cores will need modifications or adjustments.

Furthermore, linking analog IP reuse to a top-down advanced system design and verification approach is becoming an R&D challenge. A fundamental issue to cope with is the definition of adequate levels of abstraction for analog and mixed-signal behavioral descriptions able to link with digital top-down design.

In this paper, an approach to deal with these modeling requirements is proposed, and an illustrative application example is developed.

2. Analog/mixed-signal IP requirements

Analog and mixed-signal components many added problems when facing reuse of designs compared to digital circuits, or generally speaking, when comparing the automation and efficiency of the design process. The main problems derive from the fact that most parts of the analog design are developed manually and in a bottom-up approach, which requires designer time and effort together with specific skills.

The solutions that industrial and academic research are providing to handle such difficulties are based on the following concepts:

- New top-down design methodologies are needed to rise the level of abstraction of analog and mixed-signal design. The designs should begin with system-level specifications based on behavioral descriptions of the components.
- A library of (parameterized) models of the components should be used throughout the design process. These models will be available at different levels of abstraction. At the system level, they typically appear as parameterized behavioral models. They are associated with one or several detailed models at the cell-level where secondary effects, non-linearities and noise are taken into account.

- A bottom-up verification strategy is applied. The models get adapted to the different design points and they are the basis for a process of cell characterization in which the design parameters are extracted. The information obtained is back-annotated in the behavioral model, so that they can provide more realistic results in the system simulation.
- New tools and design platforms will be necessary to support these reuse methodologies.

Finally, the designer should produce exhaustive documentation in compliance with VSIA requirements [2]. The tools should support this task.

3. Case Study: a Pipeline ADC

As demonstrator of the above methodology a Pipelined Analog-to Digital Converter (ADC) with a complex digital part has been considered as mixed-signal IP. The complexity of the digital circuit derives, in this case, from the incorporation of digital correction and calibration algorithms, and from the inclusion of different testing modes for the analog part [3]. The block diagram in Fig.1 shows the basic structural subdivision carried out among the analog and digital parts of the converter. The block labelled A/D represents the analog part and block labelled DCAD represents the digital part, which controls all the operation modes of the A/D block and processes its outputs (subcodes). Both parts can be configured for a determined application by selecting the number and resolution of the basic stages comprising the A/D block, and the calibration algorithm.

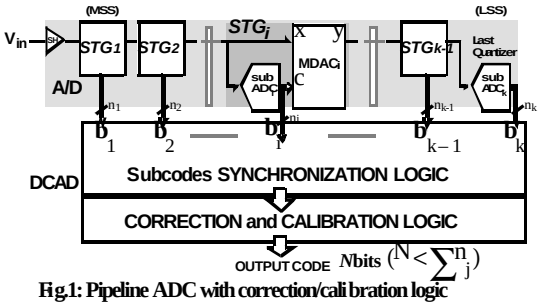

Fig.1: Pipeline ADC with correction/calibration logic

Verifying all the operation modes of the system in an early phase of design and having the possibility to quickly perform modifications (or to prove alternative calibration algorithms) leads us to develop a behavioral model of the whole system in a high-level language. This model must be simple but at the same time sufficiently precise and detailed to be able to predict static and dynamic performance. Even more, since an exhaustive set of realistic patterns coming from the analog part are needed to verify the digital part, a common simulation platform is required. These situations where a feedback loop exists between the digital and analog processes are difficult to verify using separate simulation tools.

In our case, both VHDL-AMS and VHDL are used. The DCAD block is described with fully-synthesizable VHDL. The analog block A/D can be described with VHDL-AMS, although for this specific example a VHDL modeling has been shown also possible [3].

The high-level hierarchical structure given to the A/D block for description purposes comprises the basic entities identified as SH, STGi, and the A/Dk representing the sample&hold, the converter analog stages, and the last quantizer, respectively. VHDL-AMS models have been developed which include: (i) static errors of linearity, gain and offset, and, (ii) dynamic errors mainly due to local settling errors. The parameters for defining the behavioral model were obtained from both the general specifications of the system and the circuit low–level behavior. The physical parameters can be extracted and back-annotated from electrical simulations and even from an integrated Si prototype. In our example they correspond to the case of stages programmable for 2 or 3 bits of resolution (one of these bits is always used for digital correction) and to a CMOS fully-differential switched-capacitor implementation. Specific details for the functional model of these devices can be found in [3].

4. Conclusion

The extension of design reuse methodologies to analog and mixed-signal virtual components (IP) requires a top-down methodology similar to that used for digital design. Mixed-signal behavioral modeling at adequate levels is a first step for supporting such a methodology. This paper shows this concept for a relative complex mixed-signal example.

5. References

[1] R.A. Quinnell, “Survey: Analog and Mixed-Signal Cores ”, in EETimes, April 1999.

[2] Virtual Socket Interface Alliance, “Analog/ Mixed-Signal Extension Specification (AMS 1 2.0)”, November 1999.

[3] E. Peralías, A. Acosta, A. Rueda and J.L. Huertas, “A VHDL-based methodology for the Design and Verification of Pipelined A/D Converters”. Proc. DATE2000, pp 534-537. Paris , March 2000.