Managing the SoC Design Challenge with 'Soft' Hardware

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Abstract

Panel members will discuss, from their individual perspectives, why embedded reconfigurability has become critical to the future success of systems-on-a-chip and how they are attempting to implement solutions.

The Opportunity: Implementing reconfigu- rable logic within SoCs will also help to expand and differentiate members of product families as well as extend product lifecycles and reduce design and test cycles, thus shortening product time to market. Having reconfigurability in system-on-a-chip silicon will increase design flexibility by allowing re-use of design elements to create differentiated products. Changing or revising logic elements on the fly via reconfigurability to meet changes in standards or features or to fix design errors will help avoid increasingly expensive NRE re-spins.

The Obstacles: Without reconfigurability, designers of SoCs face a growing variety of demands and obstacles.

One of the toughest demands to meet is shortening the design and test cycle in an effort to reduce product time to market. Another demand is the necessity to design for reuse. A third demand is the need to adhere to changing standards or product features. A growing obstacle is the increasing complexity of SoC design and verification. And perhaps, the biggest obstacle is the increasing cost of mask sets due to shrinks in process technology and the growing number of mask layers.

Integrating reconfigurable logic into system-level, single-chip ASICs and ASSPs is also extremely difficult to accomplish. Reprogrammable blocks of logic must be fully integrated with the standard cell. Standard ASIC design flows and methodologies must be implemented. In addition, provisions for design verification and self test of the reconfigurable blocks must be addressed.

The Controversy: How much of the reconfigurable solution should be implemented in soft IP verses physically embedded as blocks of reprogrammable core logic?