Test Generation Based Diagnosis of Device Parameters for Analog Circuits[1]

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ABSTRACT

With the increasing complexity of manufacturing processes and the shrinking of device geometries, the performance metrics of integrated circuits (ICs) are becoming increasingly sensitive to random fluctuations in the manufacturing process. We propose a diagnosis methodology that can be used to infer the cause(s) of variations in performance of analog ICs. The methodology consists of (a) a device parameter computation technique which is used to compute the device parameters of an IC from measurements made on it and (b) a cause-effect analysis module that is used to compute the cause of the variation in performance metrics of a given set of ICs. Simulation results to demonstrate the effectiveness of the technique are presented.

1. Introduction

Analog ICs are specified by a set of *performance metrics* (such as Gain, Bandwidth, THD, slew rate etc.) which are measured during production and tested against specified limits (*specifications*) to determine whether the ICs are good or bad. This process is known as specification testing. Analog ICs, in general, have many complex performance metrics that depend on a multitude of device parameters. *Parametric yield loss* is often a problem in analog IC designs, where a significant portion of ICs manufactured fail specification tests due to variations in process parameters. Usually, a large number of designs are manufactured using the same manufacturing process and the dependencies of the performance of these designs on device parameters are often different. The tuning of the process to improve the yield of one design may adversely affect the yields of other designs. Process shifts over time can also cause a reduction in yield. The dependencies of analog IC performance metrics on process fluctuations are very complex and not known in closed form. The performance metrics of an analog IC depend on the values of a set of *device parameters* of the IC (Vt, Kn, γ of transistors, resistivity etc.). In this paper, we propose a methodology through which the device parameters can be computed from measurements made on the ICs. We use the set of computed device parameters to diagnose the cause of variations in performance metrics of the ICs.

In published research, many authors [1-3] have described techniques for diagnosing process fluctuations from measured device parameters. However, since device parameters can only be measured on a few test sites on a *wafer*, these procedures cannot be used to diagnose problems caused by variation of parameters between different chips *on the same wafer*. Also, the relationship between device parameters and the performance metrics of a circuit are often not known well enough to diagnose the cause of circuit performance variations in terms of variations in device parameters. It has been shown that the device parameters which control a circuit's behavior can be computed from measurements made on the circuit, if the measurements satisfy certain *diagnosability conditions* [4, 23]. Cherubal and Chatterjee [4] have described an efficient algorithm for the computation of device parameters. In this paper, we extend the diagnosability conditions for the accurate computation of device parameters in the presence of *measurement noise*. In case these conditions are not met, we propose a technique for automatically generating optimized tests that enable the computation of device parameters. Automatic test generators for analog circuits, proposed in the literature, have been aimed at detecting discrete faults [5-10], replacing performance tests [11-15], or distinguishing specific faults from each other [16]. The new test generator proposed in this paper explicitly optimizes the ability to compute device parameters from the test response. We also propose a cause-effect analysis engine to diagnose the cause of variation in IC performance metrics in terms of the variation in device parameter values. Once the cause of parametric yield loss is diagnosed in terms of device parameters variations, the information can be used by process engineers to tune the manufacturing process to improve yield.

The rest of this paper is organized as follows. In Section 2, a description of the analog IC manufacturing and testing process is given and the need for a diagnosis tool is described. In Section 3, we give an overview of the proposed diagnosis methodology. In Section 4, we describe conditions to be satisfied by a set of measurements, for the device parameters to be identified accurately from the measurements, and describe how tests can be generated automatically that satisfy these conditions. In Section 5, the modeling tool used to approximate the relationship between the device parameters and measurements made on an IC is described. In Section 6, the process of computing device parameters from measurements made on an IC is described. In Section 7, the cause-effect analysis engine for diagnosis is described. Simulation results to validate the technique are presented in Section 8 and avenues for future research are discussed in Section 9.

2. Analog IC manufacturing and testing

Semiconductor ICs are manufactured in *lots* of *wafers*, which contain large (typically thousands) of ICs. Each wafer contains a few sites which have special test structures which enable the measurement of device parameters (Electrical Test or ET measurements). If the ET parameters are within prescribed limits, specification tests are performed on the ICs on the wafer and the 'good' ICs are diced and packaged and tested again against a full set of specifications. The limits on the ET measurements are usually set to be very wide, so that a wafer containing some good ICs

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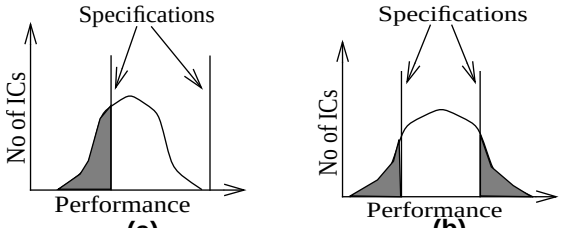

FIGURE 1. Yield Loss in ICs

is not rejected. Analog ICs often face yield problems wherein a set of the ICs on a wafer fail the specification tests, while the ET data is within limits. Two typical yield problems are shown in Figure 1(a) and Figure 1(b), which show possible histograms of performance metrics of ICs. In Figure 1(a) a shift in a process parameter causes yield loss (shaded region) while in Figure 1(b) a large variance in a performance metric causes loss in yield. These yield problems are often caused by the variation of device parameters across a wafer (i.e chip-to-chip variation in device parameters).

We model an IC manufacturing process hierarchically as

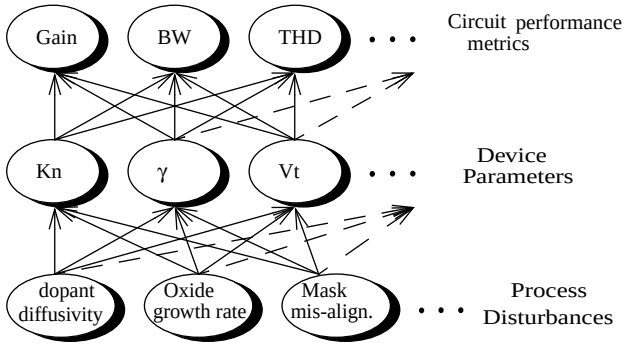

FIGURE 2. Model for Analog IC Manufacturing

shown in Figure 2. Every step in the manufacturing process is affected by a set of *process disturbances* (such as changes in diffusivity of dopants, oxide growth rates, etc.) [1] which result in fluctuations in device parameters (process outputs [1]) of ICs. The device parameters in turn control the performance metrics of ICs, which determine yield. The process disturbances cause the device parameters vary from lot-to-lot, from wafer to wafer within a lot, and from IC to IC within a wafer. The lot-to-lot and wafer-to-wafer variations can be monitored by measuring the device parameters using the wafer test structures. However, in the current manufacturing methodology there is no way of directly monitoring the variation of device parameters across ICs on a wafer. This makes the diagnosis of yield problems caused by the variation of device parameters within a wafer extremely difficult.

3. Overview

We define the device parameter diagnosis problem as follows: Given a set of analog ICs and a set of performance metrics, the proposed diagnosis approach should relate the cause(s) of any variation in the performance metrics of the ICs to the variation in device parameters.

Any measurement made on an IC for a given manufacturing process will depend on the values of a set of critical device parameters. We denote this functional dependence by

$$\bar{m} = \bar{f}(\bar{p}) \qquad \bar{m} \in \Re^{n_p} \qquad \bar{p} \in \Re^{n_m} \tag{1}$$

where $\bar{m}$ is a set of measurements made on the IC, $\bar{p}$ is the set of device parameters, n_p is the number of device parameters and n_m is the number of measurements. This functional relationship is usually not known in closed form and is evaluated using circuit simulation. Given the set of measurements made on an IC, we solve for the set of device parameter values of the IC using iterative numerical techniques. This can be computationally very expensive for large IC designs due to excessive simulation times, as the functional dependence given in Equation 1 has to be evaluated using circuit simulation. Cherubal and Chatterjee [4] have shown that it is possible to approximate the functional dependency in Equation 1 using nonlinear regression techniques. This replaces computationally expensive circuit simulation with function evaluations, thereby reducing the cost of computing device parameters. The regression models are built using a training technique requiring repeated circuit simulation, and incurs a one-time simulation cost. In this paper, we propose methods to automatically generate tests to aid diagnosis. Techniques for relating yield problems to the variation in device parameters are proposed.

An overview of the proposed methodology is shown in

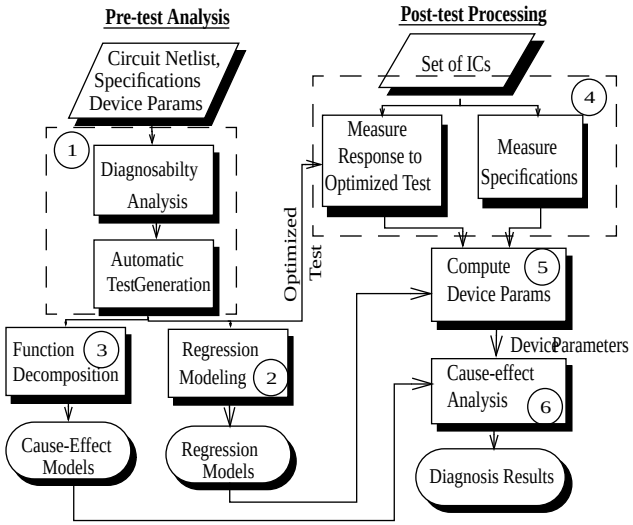

FIGURE 3. Overview of Diagnosis Methodology

Figure 3. It consists of pre-test analysis and post test processing. The methodology consists of the following steps.

1. A diagnosabilty analysis is performed to see if the device parameters can be accurately computed from the set of performance metrics of the IC. If this is not possible, optimized test stimuli are generated which allow the unique identification of device parameters that can cause yield problems.
2. Non-linear regression models are built, which relate the performance metrics and the optimized test response of the IC to the device parameters. These regression models are used to solve for the values of device parameters of ICs from their response to the optimized test stimuli.

3. To diagnose yield problems, we would like to identify the contribution of each device parameter to variation in performance of ICs. Therefore, the regression models for the performance metrics are decomposed to the individual model components pertaining to each device parameter and those due to interaction between parameters.
4. During the post-test phase, when there is observed yield loss for an IC design, the optimized tests are applied to a set of ICs having yield problems and their response is measured.
5. The device parameters for each individual IC are computed from their responses to the optimized test.
6. Using the decomposed regression models from step 3, the effect of the computed device parameter variations on the performance of the ICs is analyzed.

4. Diagnosability Analysis and Test Optimization

In order to diagnose the cause of variation in performance metrics of an IC, we need to compute the device parameters of every IC from measurements made on it. We use sensitivity based heuristics to check if the parameters can be uniquely computed from the set of performance metrics for a given IC. If the parameters cannot be uniquely determined from the set of performance metrics, tests are automatically generated that will facilitate the accurate computation of IC device parameters. The automatic test generator consists of a *test cost function* which is used to evaluate the goodness of a test and a *search algorithm* for finding the optimal test stimulus. The automatic test generator uses a Genetic Algorithm (GA) based optimization procedure for finding the optimal stimulus. GA has been used to find globally optimal solutions for complex search and optimization problems with many local minima [18]. GAs have been used for test generation in analog circuits for fault isolation [16] and fault detection [11]. In Section 4.1, the conditions for the accurate computation of device parameters from measurements made on an IC are described. In Section 4.2, the test cost function that is used to evaluate the goodness of test stimuli is described. In Section 4.3, the genetic algorithm used to search for the optimal test stimulus is described.

4.1 Diagnosability Analysis

Liu et. al [23] have shown that the number of parameters of a circuit that can be uniquely solved for, from a set of measurements made on the circuit is given by

$$n_d = rank(\mathbf{S}) \tag{2}$$

where $\mathbf{S}$ is the sensitivity matrix given by

$$\mathbf{S} = \begin{bmatrix} \frac{\partial m_1}{\partial p_1}\cdot p_1 & \frac{\partial m_1}{\partial p_2}\cdot p_2 & \cdots & \frac{\partial m_1}{\partial p_{n_p}}\cdot p_{n_p} \\ \frac{\partial m_2}{\partial p_1}\cdot p_1 & \frac{\partial m_2}{\partial p_2}\cdot p_2 & \cdots & \frac{\partial m_2}{\partial p_{n_p}}\cdot p_{n_p} \\ \cdots & \cdots & \cdots & \cdots \\ \frac{\partial m_{n_m}}{\partial p_1}\cdot p_1 & \frac{\partial m_{n_m}}{\partial p_2}\cdot p_2 & \cdots & \frac{\partial m_{n_m}}{\partial p_{n_p}}\cdot p_{n_p} \end{bmatrix} \tag{3}$$

The rank of a matrix is given by the number of its *non-zero singular values*. However, the parameters cannot often be computed accurately even though the condition in Equation 2 is satisfied, due to the effects of measurement noise. Therefore, we will analyze the effect of measurement noise on the errors in the computed values of parameters. Let each of the measurements in $\bar{m}$ be affected by measurement noise $\bar{e}_m$ having a variance of σ_m^2. If different measurements have different variances in measurement noise, the measurements can be normalized, so that they all have the same variance in measurement noise. In the presence of noise, Equation 1 becomes

$$\bar{m}_o + \bar{e}_m = \bar{f}(\bar{p}_o + \Delta\bar{p}) \tag{4}$$

where $\bar{m}_o$ and $\bar{p}_o$ are the true (noise-free) values of measurements and parameters respectively. Assuming that the measurement noise is small, the error can be approximated by a linear function about $\bar{p}_o$ to get $\bar{f}(\bar{p}_o + \Delta\bar{p}) = \bar{f}(\bar{p}_o) + \mathbf{S}\cdot\frac{\Delta\bar{p}}{\bar{p}}$. Noting that $\bar{m}_o = \bar{f}(\bar{p}_o)$, we get,

$$\mathbf{S}\cdot\frac{\Delta\bar{p}}{\bar{p}} = \bar{e}_m \tag{5}$$

The effect of measurement noise can be analyzed using the *Singular Value Decomposition* (SVD) [17] of $\mathbf{S}$. SVD decomposes a matrix into the product of 3 matrices as

$$\mathbf{S} = \mathbf{U}\cdot\Sigma\cdot\mathbf{V}^{\mathrm{T}} \tag{6}$$

where $\mathbf{U}$ and $\mathbf{V}$ are *orthonormal* matrices ($\mathbf{U}^{\mathrm{T}}\cdot\mathbf{U} = \mathbf{I}$, $\mathbf{V}^{\mathrm{T}}\cdot\mathbf{V} = \mathbf{I}$ where $\mathbf{I}$ is the identity matrix) and Σ is a diagonal matrix with decreasing positive diagonal elements. Substituting Equation 6 into Equation 5 and noting that $\mathbf{U}^{\mathrm{T}}\cdot\mathbf{U} = \mathbf{I}$ and $\mathbf{V}^{\mathrm{T}}\cdot\mathbf{V} = \mathbf{I}$, we get

$$\frac{\Delta\bar{p}}{\bar{p}} = \mathbf{V}\cdot\Sigma^{-1}\cdot\bar{e}'_m = \sum_{i=1}^{n_p}\bar{V}_i\cdot\frac{e'_{mi}}{\Sigma_i} \tag{7}$$

where $\bar{e}'_m = \mathbf{U}^{\mathrm{T}}\cdot\bar{e}_m$, $\bar{V}_i$ is the i^{th} column of $\mathbf{V}$, e'_{mi} is the i^{th} element in $\bar{e}'_m$ and Σ_i is the i^{th} diagonal element of Σ. Since $\mathbf{U}$ is orthonormal, it can be shown that the variance of $\bar{e}'_m$ is σ_m^2. Computing the *expected sum of squared errors* in device parameters, we get

$$E\left(\sum_{i=1}^{n_p}\left(\frac{\Delta p_i}{p_i}\right)^2\right) = \sum_{i=1}^{n_p}\frac{\sigma_m^2}{\Sigma_i^2} \tag{8}$$

where $E(\ )$ is the expectation operator. Now if we want the L.H.S of Equation 8 to be less than a pre-defined constant, K, (i.e. we want the average squared error in computed parameters to be less than K/n_p) the number of parameters that can be solved for from the given set of measurements is

$$n_d = max(n) \text{ s.t. } \sum_{i=1}^{n}\frac{\sigma_m^2}{\Sigma_i^2} < K \tag{9}$$

The condition given in Equation 9 is based on differential sensitivity, which is valid only for small changes in parameters. Therefore, Equation 9 has to be evaluated at *every point in the device parameter space* (the space spanned by the range of possible variations of parameters) for ensuring diagnosability. However, this may prove to be computationally too expensive.

Therefore we use the heuristic of evaluating Equation 9 only for the *nominal values of parameters* as an estimate of diagnosabilty.

4.2 Test Cost Description

Any automatic test generation algorithm needs a test cost that can be used to compare the goodness of tests during optimization. The tests that we need are such that, when augmented with the performance measurements, will enable the accurate computation of device parameters. Therefore we start with the augmented sensitivity matrix, given by

$$\mathbf{S} = \begin{bmatrix} \mathbf{S}_p \\ \mathbf{S}_n \end{bmatrix} \tag{10}$$

where $\mathbf{S}_p$ is the sensitivity matrix of the performance measurements and $\mathbf{S}_n$ is the sensitivity matrix of the newly generated test. An SVD is performed on $\mathbf{S}$ and the singular values Σ_i are computed. Since we are trying to minimize the error in the values of computed parameters, Equation 8 can be used as a cost function to be minimized. However, this has a tendency to be dominated by a few small Σ_i, (large values of $1/\Sigma_i^2$) resulting in poor quality tests being generated. Therefore, we have used the following as a cost function to be maximized.

$$C = \sum_{i=1}^{n_p} \mathrm{sat}\left(\frac{\Sigma_i^2}{\Sigma_{max}^2}\right) \qquad \mathrm{sat}(x) = \begin{cases} x & x < 1 \\ 1 & x \geq 1 \end{cases} \tag{11}$$

where Σ_{max} is a constant related to the minimum accuracy in computed parameters, K. This cost function maximizes the singular values, which has the same effect as minimizing the reciprocals of the singular values. A saturating function sat( ) is applied to Σ_i so that the cost function cannot be dominated by a few, large, singular values.

4.3 Genetic Algorithms for Test Optimization

GAs are stochastic optimization algorithms which encode a given problem into a genetic string or chromosomes, and perform operations similar to evolution for optimization. GAs maintain a set of potential solutions to the given problem from which new solutions are created by the genetic operations of *selection*, *crossover* and *mutation*. We have used piece-wise linear (PWL) transient waveforms as the test signals being optimized. PWL waveforms have shown great promise in automatic test generation for replacing performance tests [11-13] and for distinguishing failure modes [16]. This optimization process is general and can also be applied to other types of waveforms such as multi-frequency tests. A more detailed description of using GA for optimizing PWL waveforms can be found in the paper by Variyam and Chatterjee [11].

5. Regression Modeling

We use nonlinear regression modeling techniques to create a piece-wise polynomial function that relates the device parameters to measurements made on the Device-Under-Test (DUT). We have used a popular regression modeling tool MARS [20] for this purpose. MARS is able to model nonlinear functions with a large number of independent variables and can adapt to the degree of nonlinearity of the function being modeled. MARS has been used for statistical fault simulation [22] test generation [11] and parametric fault diagnosis [4]. MARS produces piece-wise polynomial functions of the form

$$y = \sum_{i=1}^{M} a_i B_i(\bar{\boldsymbol{x}}) \tag{12}$$

where $B_m(\bar{\boldsymbol{x}})$ are basis functions which are products of simple first order spline functions. A more detailed description of the technique can be found in the original paper by Friedman [20].

The regression models are built using a set of training data generated using simulation. In this process, a set of parameter variations are randomly generated and measurements on the IC are simulated using the generated parameter variations. This set of parameter variations and simulated measurements are used to build the regression model given in Equation 12.

6. Computing Process Parameter Values

Cherubal and Chatterjee [4] have shown that it is possible to solve for the parameter values of the DUT from measurements made on it. We have followed a similar approach in this paper. A *Newton-Raphson* (N-R) iterative procedure [4] is used to solve for the parameters. A step in the N-R iteration consists of

$$\bar{\boldsymbol{p}}_{i+1} - \bar{\boldsymbol{p}}_i = \mathbf{J}(\bar{\boldsymbol{p}}_i)^{-1} \cdot (\bar{\boldsymbol{m}} - \bar{\boldsymbol{f}}_{pm}(\bar{\boldsymbol{p}}_i)) \tag{13}$$

where $\bar{\boldsymbol{p}}_i$ and $\bar{\boldsymbol{p}}_{i+1}$ are the guesses for the parameter values and $\mathbf{J}(\bar{\boldsymbol{p}}_i)$ is the *Jacobian* of $\bar{\boldsymbol{f}}_{pm}(\bar{\boldsymbol{p}})$ at $\bar{\boldsymbol{p}}_i$. We use the regression models that relate the measurements made on the CUT to the parameters to evaluate $\bar{\boldsymbol{f}}_{pm}(\bar{\boldsymbol{p}})$ and $\mathbf{J}(\bar{\boldsymbol{p}}_i)$. This reduces the complexity of solving Equation 1. It may not always be possible to compute all the parameters accurately from the test responses. Parameters groups among which parameters cannot be uniquely identified are called *ambiguity groups* [23]. In case ambiguity groups exist, they are identified using the technique described by Liu et. al. [23] and *one* possible solution for the parameter values is computed.

7. Cause-Effect Analysis

The regression model output of MARS can be decomposed to identify the contributions of different input parameters to the model. This analysis is described as ANOVA (ANalysis Of VAriance) decomposition by Friedman [20]. This analysis is the decomposition applied to a *function*, is different from the classical ANOVA analysis in statistics [21]. The ANOVA decomposition resolves $f_{pm}(\bar{\boldsymbol{p}})$ into a set of functions in the form

$$f_{pm}(\bar{\boldsymbol{p}}) = \sum_i f_i(p_i) + \sum_{i,j} f_{i,j}(p_i p_j) + \sum_{i,j,k} f_{i,j,k}(p_i p_j p_k) + \ldots \tag{14}$$

where the first sum give the contributions of individual variables, the second sum gives the contributions due to two variable interaction, and so on. Given a set of diagnosed parameters for a set of ICs, the individual component functions in the ANOVA decomposition (f_i, $f_{i,j}$, ...) can be evaluated to compute the contribution of each parameter and that of parameter interactions on the variation in IC performance. To compute the effect of a parameter p_i, the mean and variance of $f_i(p_i)$ are estimated using

$$\hat{m}_{p_i} = \frac{1}{N} \sum_{j=1}^{N} f_i(\hat{p}_{i,j}) \tag{15}$$

$$\hat{\sigma}^2_{p_i} = \frac{1}{N-1}\sum_{j=1}^{n}(f_i(\hat{p}_{i,j}) - \hat{m}_{p_i})^2 \quad (16)$$

respectively, where $\hat{p}_{i,j}$ is the computed value of p_i for IC number j. The mean and variance of effects due to interactions between parameters is estimated in a similar way using $f_{i,j}$.

8. Results

In this section, we apply our methodology to a CMOS opamp described in the ITC mixed-signal test benchmarks [24]. All experiments were done on a 350MHz Sun-Ultra-10 workstation. The diagnosability of device parameters for the circuit was analyzed and tests were generated to aid the computation of device parameters as described in Section 4. Regression models were built relating the device parameters to the output response of the circuit as described in Section 5. 400 circuit simulations were needed to create the regression models, which took 1.2 hours of CPU time. The results for diagnosis are given in two sections. In Section 8.1, we demonstrate the computation of device parameters from the automatically generated tests and performance measurements. This is done by simulating random variations in *all* device parameters of the opamp for a set of devices, and then computing the device parameters from the test response. In Section 8.2, the cause effect analysis methodology is analyzed using a simulated scenario, where a shift in the mean value of device parameters (process shift) and increased variance in device parameters (poor process control) cause yield loss. The cause-effect analysis method is shown to correctly diagnose the cause of yield loss.

8.1 Device Parameter Computation Results

The schematic diagrams for the CMOS opamp is shown in Figure 4. The process parameter variations for the opamp are

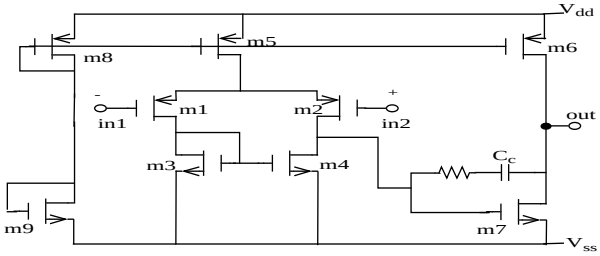

FIGURE 4. MiST Benchmark opamp

shown in Table 1. Performance tests for the opamp included offset

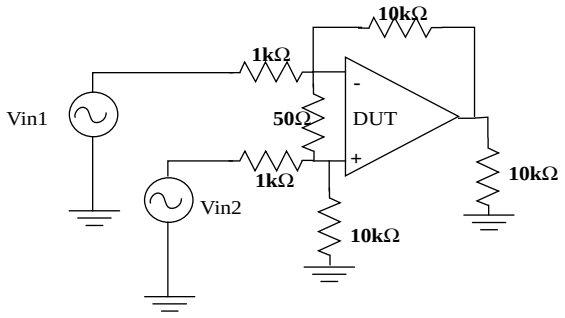

FIGURE 5. Test Configuration for CMOS opamp

voltage, slew rate, large signal gain, CMRR and PSRR. Accurate computation of device parameters was not possible from the performance tests alone. Alternate tests were generated for the CMOS opamp using the circuit configuration shown in Figure 5. This test configuration was first described by R. Pease [25] for the measurement of CMRR for opamps. The optimized tests and nominal circuit response for the CMOS opamp are shown in Figure 6. The test response was sampled at a frequency of 100

TABLE 1. Device parameters for CMOS opamp

Parameter	Max	Min	Parameter	Max	Min
xl_p	0.3 µm	-0.3 µm	xl_n	0.3 µm	-0.3 µm
xw_p	0.3 µm	-0.3µm	xw_n	0.3 µm	-0.3 µm
ld_p	0.03µm	0.1µm	ld_n	0.03µm	0.1 µm
Vt_p	-0.65 V	-1.05 V	Vt_n	0.60 V	1.0 V
γ_p	$0.2\sqrt{V}$	$0.6\sqrt{V}$	γ_n	$0.3\sqrt{V}$	$0.8\sqrt{V}$
tox_p	225 A°	275 A°	tox_n	225 A°	275 A°
Cc	1.1 pF	0.9 pF	Rc	2.5kΩ	1.5kΩ

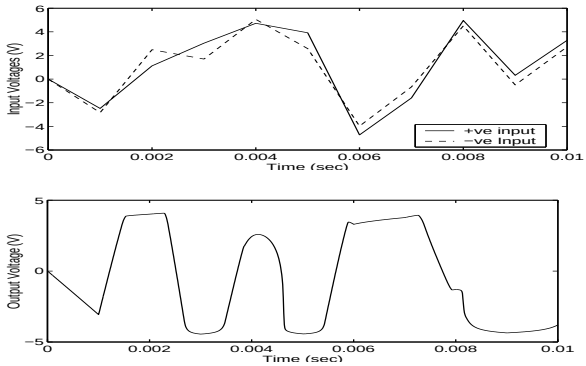

FIGURE 6. Optimized test and Response for CMOS opamp

kHz to form the alternate test measurements. A measurement noise of 6mV peak-to-peak was assumed for the transient response and that of 1mV peak-to-peak for DC measurements. To test the device parameter computation technique, random circuit instances were generated by varying all the device parameters of the circuit. Measurement noise was simulated by adding Gaussian distributed random numbers to the simulated test responses. Device parameter computation was attempted from the simulated test responses. The comparison of the simulated and computed parameters for the device parameters of the opamp is given in Figure 7. The 'true' (simulated) value for each parameter is given by the straight line while the computed values for the device parameters are marked by '+' signs. The device parameter computation algorithm is able to compute all but 4 parameters (Rc, ld_p, ld_n, xw_p) accurately. It is seen that the computed parameters track the simulated parameters, proving the effectiveness of the generated test and the device parameter computation algorithm. The CPU time required to compute the device parameters from the test response was 29.1 milliseconds per IC.

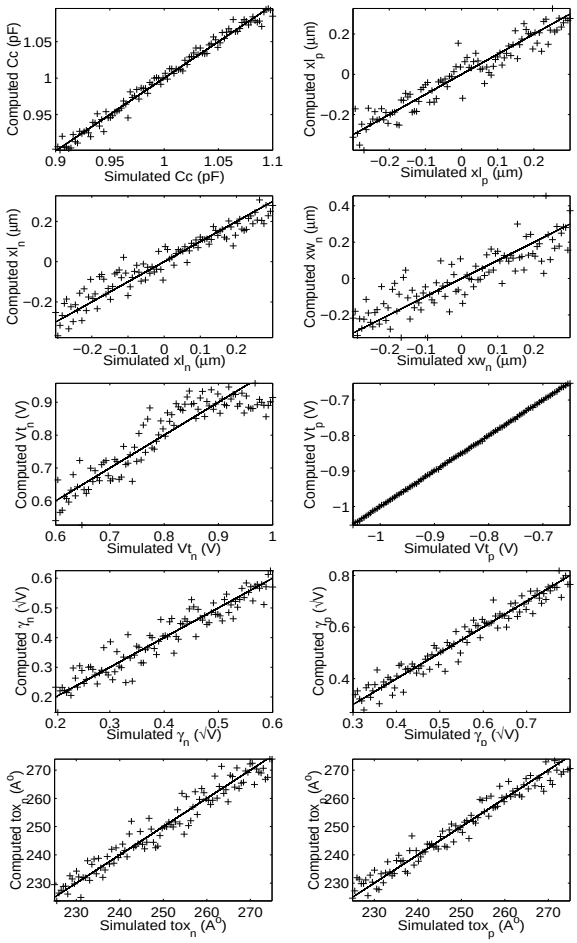

FIGURE 7. Comparison of Simulated and Computed Device Parameters for CMOS opamp

8.2 Cause-Effect Analysis

To study the effectiveness of the cause effect analysis two case

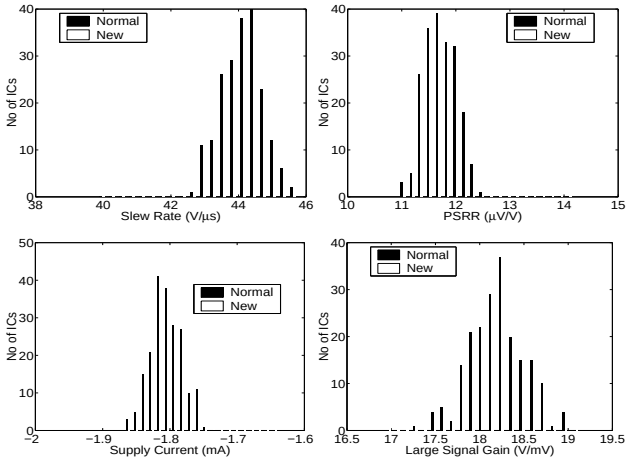

FIGURE 8. Effect of change in Device Parameters om Opamp performance metrics

studies were performed. In the first case, a Monte Carlo simulation of the circuit was performed to generate a set of IC instances and

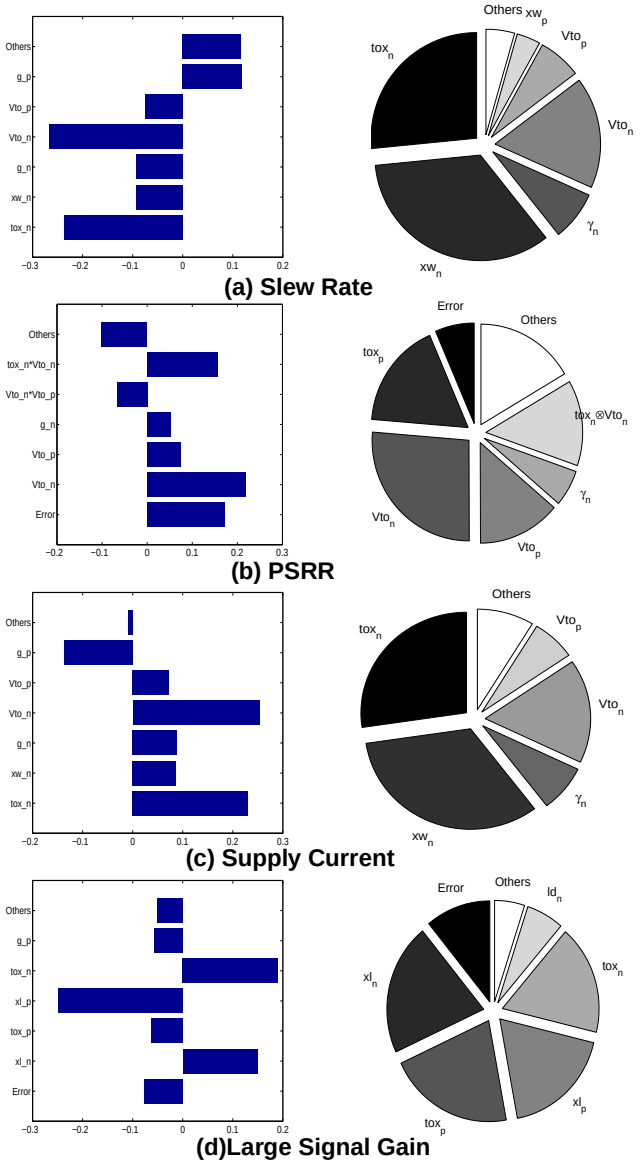

FIGURE 9. Cause Effect Analysis for performance metrics of CMOS opamp

the performance metrics of these ICs were measured. This was considered the nominal statistical distribution of device performance. In the second case, circuit instances were generated with change in nominal values and increased variances introduced into all the device parameters to simulate a process shift and poor control of process, respectively. (Note that this is a realistic scenario, as a fluctuation in a process parameter typically affects multiple device parameters). This is considered the new or faulted distribution of device performance. It was found that 4 of the opamp's performance metrics, namely, slew rate (SR), supply current (I_{sup}), power supply rejection ratio (PSRR) and large signal gain (A_v) were affected by this change in device parameter statistics. The histograms of the normal and faulted IC performance metrics are shown in Figure 8. The device parameter values for the faulted

set of ICs were computed as described in Section 6. The cause-effect analysis was performed on the second set of ICs to diagnose the cause(s) of drift and increased in variance of performance metrics. The results of cause-effect analysis on the affected ICs is shown in Figure 9. The bar-graphs on the left side of Figure 9(a), (b), (c) and (d) show the relative contributions of various device parameters to the *drift in performance metrics*. It can be seen that the shift (reduction) in slew rate is mainly due to the shifts in the device parameters tox_n and Vt_n. Therefore, those parameters must be tuned to improve the slew-rate of the set of ICs. Similar inferences may be made about the shift in supply current. The pie-charts on the right of Figure 9(a) (b), (c) and (d) show the relative contributions of each device parameter variation to the variance of each performance. For example, it can be seen that the major portion of the variance in slew rate is caused by the variation in tox_n and xw_n. Better control of these parameters is required to reduce the variance in slew rate. The portion of the bar-graphs pie-charts labeled 'Error' refers to the part of the variation that could not be explained by the variation in any of the parameters considered. It is seen that the technique is able to diagnose a major portion of the cause of shift and variance in circuit performance parameters. The technique is able to track variation in performance caused by the interaction between parameters as can be seen from Figure 9(b) (a significant portion of the variance in PSRR is caused by the $tox_n \times Vto_n$). This information can be used to provide feedback to process engineers to tune the manufacturing process to improve yield.

9. Conclusions

In this paper, a methodology for diagnosing yield problems in analog ICs has been demonstrated. Simulation results show the effectiveness of the proposed technique. Future work will involve verifying the methodology for larger circuits in a real production environment.

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