CMOS Open Defect Detection by Supply Current Test

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Abstract

In this paper, a new test method is proposed for detecting open defects in CMOS ICs. The method is based on supply current of ICs generated by applying time-variable electric field from the outside of the ICs. The feasibility of the test is examined by some experiments. The empirical results promised us that by using the method, open defects in CMOS ICs can be detected by measuring supply current which flows when time-variable electric field is applied.

1. Introduction

Most of the defects generated in CMOS ICs manufactured by means of the state-of-art technology are shorts and opens[1]. Open defects can generate very complicated faulty effects and are very difficult to be detected[2,3,4].

As for short defects, it is well-known that supply current tests like IDDQ test are very effective and useful, since short defects are modeled as bridging faults in logic circuits and bridging faults are very difficult to be detected by measuring logic values of the primary output terminals.

On the other hand, it is very difficult to detect open defects by measuring supply current of ICs. Open defects can be classified into 2 types[5]. The one is a floating gate fault. The other is an open source/drain fault. As for floating gate faults, some kinds of test methods have been proposed[2,3,4].

Extremely large quiescent supply current change may not be always generated when an open defect is excited. Thus, it leads to the difficulty of detection by IDDQ testing[5].

It is reported that supply current test methods for detecting open defects based on dynamic or transient current of ICs are effective[6]. Some researchers attempted to develop supply current test methods based on dynamic or transient current of ICs[5,6,7,8]. The method in [7] is based on the number of the supply current peaks generated when output changes in each CMOS gate. The test methods in [5], [6] and [8] are based on the change of the transient supply current waveform generated by open fault excitation. Some researchers attempted to detect open defects by the change in the frequency domain[9,10] However, it is very difficult to measure dynamic current waveforms of ICs preciously and the waveforms can be changed by various kinds of factors, for example, unit-to-unit variation in the characteristic between supply voltage and supply current among ICs, used test setup and noise generated in the supply current measurements. It leads that it is very difficult to detect ICs having open defects with the test methods based on dynamic supply current of ICs in the practical tests.

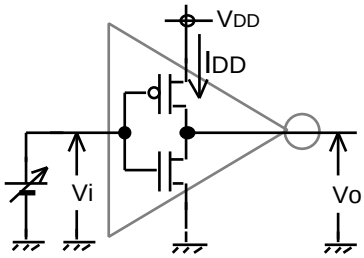
In this paper, we propose a new supply current test method for detecting open defects in CMOS ICs. The method is for detecting them by measuring supply current which flows when time-variable electric field is applied to the IC to be tested. If any open defects do not occur, large supply current will not flow when the electric field is applied to the IC. If an open defect occurs, large supply current will be generated by the applied electric field. This property is used for detecting open defects in ICs.

In section 2 and 3, the principle of our fault detection method and our test method are described, respectively. The feasibility of our test is examined by some experiments. The result is shown in section 4.

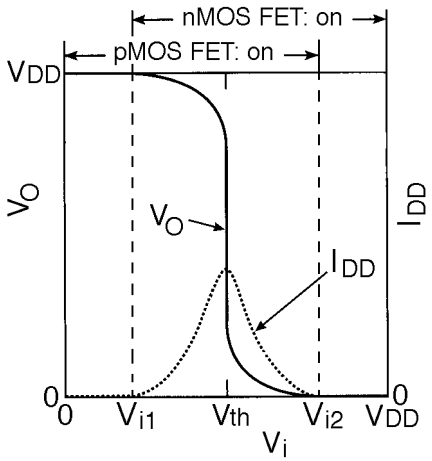
2. Principle of open defect detection

Input/output voltage characteristic of a CMOS inverter gate is shown in Fig.1. As shown in Fig.1(b), when V_i is either V_{DD} or GND, almost zero supply current will flow into CMOS inverter gates. If any shorts occur among more than one interconnection, a large quiescent supply current will flow. The property is used for detecting bridging faults in IDDQ test.

On the other hand, even if an open defect occurs in a CMOS circuit and is sensitized, large quiescent supply current may not always flow into the circuit. It leads that open defects are difficult to be detected by measuring supply current.



(a)Measurement Circuit



(b)DC characteristic curve

Fig.1 DC characteristics of CMOS inverter gate.

All nodes in a CMOS circuit are connected to either the VDD line or the GND one in operation when any open defects do not occur in it. A NAND gate circuit is shown in Fig.2. When a=b=H, nodes N1, N2 and N3 are connected to the VDD line, while N4 and N5 are connected to the GND line.

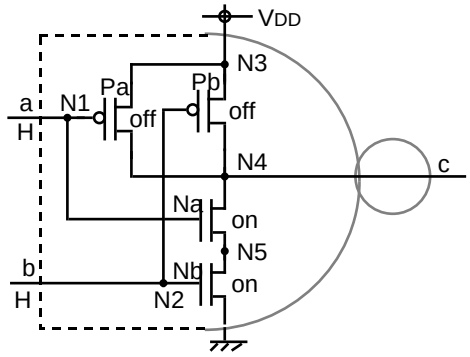


Fig.2 NAND gate circuit.

When an open defect occurs between the node N1 and the gate terminal of the nMOS transistor Na, the node N4 may not be connected to the GND line. Also, when an open defect occurs between the node N1 and the gate terminal of the pMOS Pa, the fault will generate behavior of a sequential circuit. For example, the input vector of a=b=H generates L output at the signal line c. After that, when the input vector of a=L and b=H is provided to the gate, pMOS transistor Pa can not turn on and the output maintains L level. On the other hand, when the input vector is provided after the input vector of a=b=L, H level output will be generated at the signal line c. It means that the open defect generates the output which is generated by providing the last input vector.

Since the combinational circuit reveals an operation of a sequential circuit, it is very difficult to detect it by measuring output logic values, that is, by voltage testing. Also, when an open defect occurs in an interconnection between the output terminal of a gate and an input terminal of another gate, it can not be estimated preciously what logic value will be propagated. Thus, it is difficult to generate test input vectors of voltage testing for open defects.

In this paper, such open defects in a CMOS IC are attempted to be detected by applying time-variable electric field from the outside of the IC as shown in Fig.3. If time-variable electric field is provided to the IC, the voltage of a signal line having an open defect will change in time. For example, when the open defect of F1 occurs in an inverter gate and time-variable electric field is applied as shown in Fig.4(a), the gate voltages of nMOS and pMOS transistors will change with the electric field.

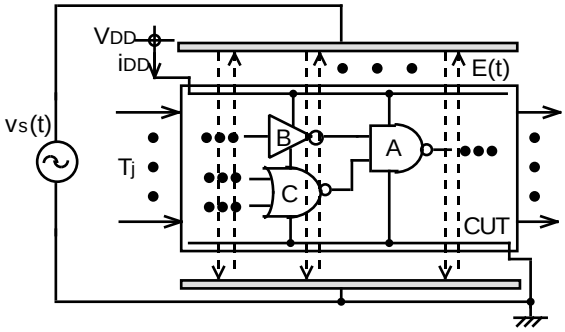
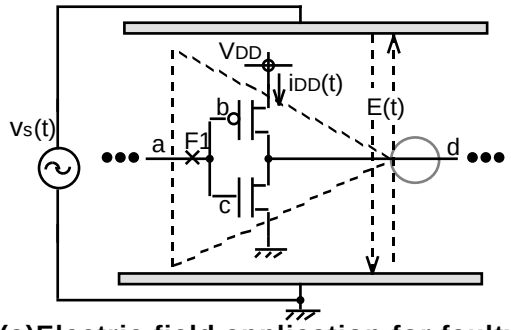
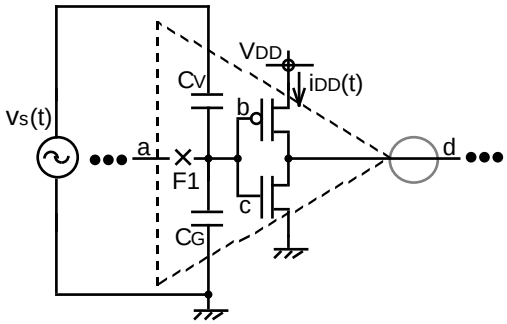


Fig.3 Open fault sensitization by electric field application.

The equivalent circuit for the circuit in Fig.4(a) is shown in Fig.4(b). By the change of the electric field generated by $v_s(t)$, the gate voltages of pMOS and nMOS transistors in the inverter gate will change in time. If the induced voltage is in the range where both the nMOS transistor and the pMOS one turn on, supply current will flow through the transistors. The range corresponds to the range between $V_i=V_{i1}$ and $V_i=V_{i2}$ in Fig.1(b) in the case of the inverter gate in Fig.1(a). The supply current change which is generated by the voltage induced by the electric field is used in our test.



(a)Electric field application for faulty gate



(b)Equivalent circuit

Fig.4 Electric field application for faulty inverter gate.

3. Open defect detection

By applying time-variable electric field from the outside of the IC to be tested, large supply current will be generated. In order to examine it, we make a faulty IC having an open defect by making a hole in a fault-free 74HC00 IC with a drill. The photograph is shown in Fig.5. The hole is made near the first pin of the IC.

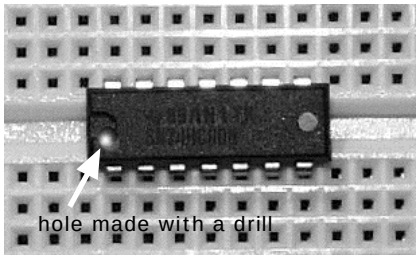


Fig.5 Photograph of 74HC00 inserted open defect manually.

When the primary input vector in Fig.6 and time-variable electric field are provided to the faulty IC, supply current $i_{DD}(t)$ of the IC is measured with a current probe. Also, supply current is measured of an unfaulty 74HC00 IC when the input vector and the electric field are provided. The results are shown in Fig.7. As shown in Fig.7, by applying electric field to the IC having the open defect, supply current flows which is different from $i_{DD}(t)$ of the unfaulty IC.

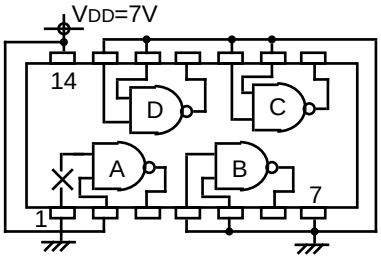
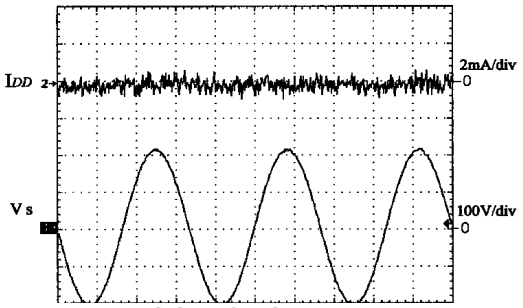
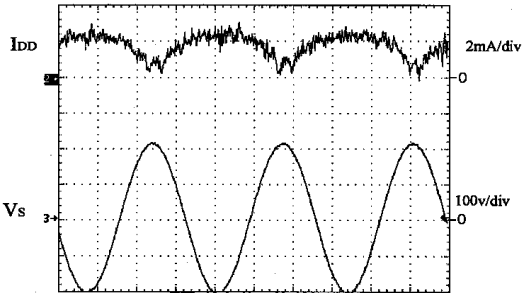


Fig.6 Circuit for testing faulty IC in Fig.5.



(a)Unfaulty IC



(b)Faulty IC in Fig.5.

Fig.7 $i_{DD}(t)$ waveform of the circuit in Fig.6.

The supply current of more than 2mA flows in Fig.7(b), which is larger than the unfaulty IC. Thus, it is expected from Fig.7 that open defects can be detected by Eq.(1), that is, by examining whether large supply current flows.

$$i_{DD}(t) > I_{th} \quad (1)$$

where I_{th} is a threshold value, which is determined by the variation of $i_{DD}(t)$'s of unfaulty ICs.

Also it is apparent from Fig.7 that the root mean square value(I_{DDC}) of $i_{DD}(t)$ in the faulty IC is different from the one(I_{DDN}) in the unfaulty IC. Thus, it is expected that open defects can be detected by means of root mean square values of $i_{DD}(t)$, that is, by Eq.(2).

$$I_{DDC} - I_{DDN} > I_{thrms} \quad (2)$$

where I_{thrms} is a root mean square value and is used as a

threshold value which is determined by the variation of $i_{DD}(t)$'s of unfaulty ICs.

Furthermore, the component of the same frequency as $v_s(t)$, that is, 3kHz, appears only in the faulty supply current waveform. Thus, the power spectrum obtained by frequency domain analysis method can be used for the detection.

4. Experimental evaluation

In order to examine the feasibility of our test, we developed a test system. By using the system, the feasibility is examined experimentally.

4.1 Developed test setup

In order to generate high power electric field, we developed a $v_s(t)$ generation circuit. The circuit consists of a voltage source which can generate a sine waveform and a voltage amplifier circuit. The gain of our developed amplifier circuit is about 200 and by using the circuit, a sine waveform of up to 300Vp-p can be generated.

As for the electrodes, sheet copper is used. The configuration in our experiments is shown in Fig.8(a). A piece of cellophane sheet is inserted between the IC to be tested and the sheet copper. It is located upon the IC as shown in Fig.8(b). The top view photograph is shown in Fig.9.

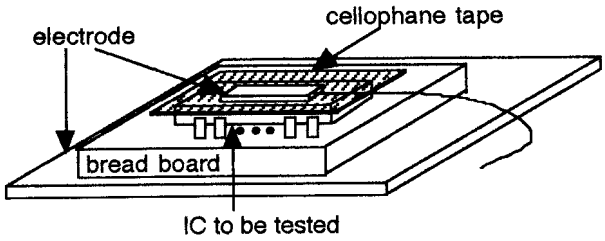
4.2 Supply current generated by open defects

It has been impossible for us to get commercial LSIs having open defects. Thus, 2 kinds of SSIs are used in our experiments.

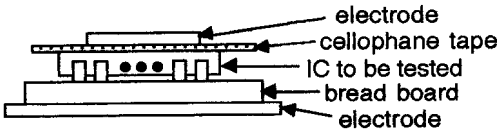
The one is a NAND gate IC(74HC00), which is shown in Fig.5. The measured supply current waveform is shown in Fig.7(b). As shown in Fig.7, the single open fault can be detected by measuring the supply current. When L level is provided to the second pin of the 74HC00 IC, even if the electric field is applied, large supply current did not flow. The reason is apparent from Fig.2. Any current paths from VDD to GND can not be generated since Nb continues to be in the cut-off state by providing b=L. It means that test vectors for our test method should be prepared before testing.

The other is a bus driver IC(74HC245). The test input vector is provided to the IC which is shown in Fig.10(a). Usually, the input vector of DIR=L and $\overline{G}$=H is inhibited. However, in our experiments, the input vector is provided to the IC in order to generate the same phenomena as open defects in it.

The equivalent circuit of a 3-state inverter gate[11] is shown in Fig.10(b). By providing the input vector shown in Fig.10(a) to the IC, the same effects as two open defects OF1 and OF2 can be generated.



(a)Configuration



(b)Side view

Fig.8 Our test board for open fault detection

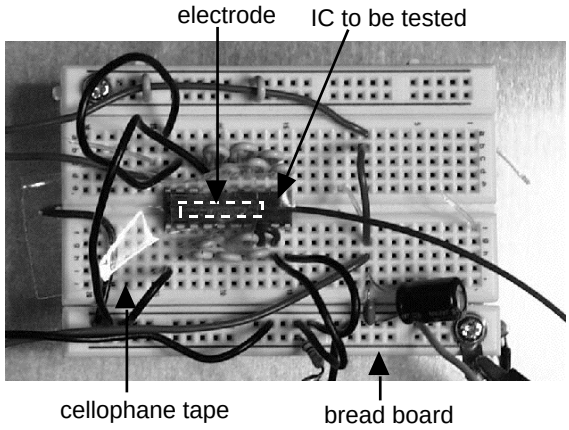
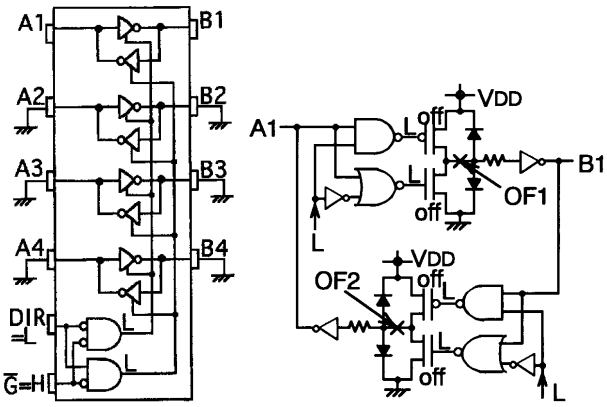


Fig.9 Photograph of our setup for open fault detection.



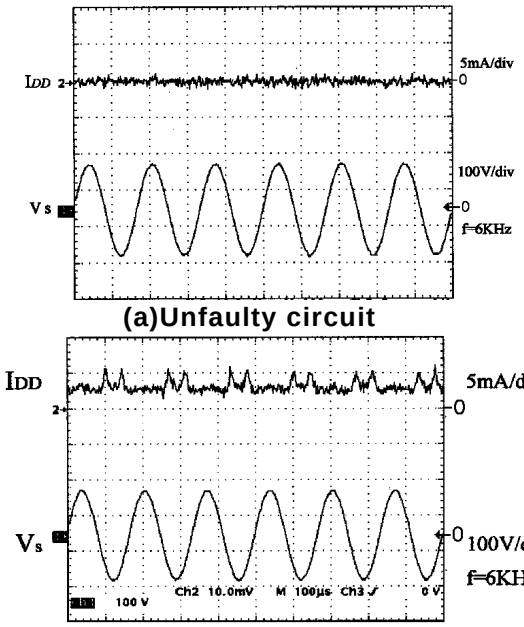
(a)Test inputs (b)Equivalent circuit

Fig.10 Generation of open defects.

The measured waveforms are shown in Fig.11. From the waveforms in Fig.7 and Fig.11, it is expected that open defects in CMOS ICs can be detected by our method.

In our experiments, very simple electrodes are used as shown in Fig.8 and Fig.9. The shape of the electrodes can be optimized. By optimizing it, larger supply current change will be generated.

The test speed of our test method will not depend on the frequency of applied electric filed, but will depend on how long time is required to induce voltage at an open node, with which large supply current can be generated. The time will depend on layout of a targeted IC and IC process parameters used in the fabrication. We think that our test speed will be faster than IDDQ test method.



(a)Unfaulty circuit

(b)Circuit having 2 open nodes

Fig.11 Open fault detection for bus driver IC.

5.Conclusions

In this paper, a new supply current test method is proposed for detecting faulty IC's having open defects. The feasibility of the test is examined by some experiments for SSIs having open defects inserted mechanically or electrically. In this paper, the test method has not been applied to the tests of any commercial LSIs. However, the experimental results in this paper promise us that open defects in CMOS ICs will be detected by measuring the supply current which flows when time-variable electric field is applied.

Until now, any test methods for open defects in CMOS ICs have not been proposed, which are applicable for the practical tests. Since this method is based on the voltage change of a faulty signal line induced by an electric filed stimulus from the outside of ICs, robust testability will be obtained.

Test input vectors for our test method should be prepared before testing. It is one of our future works to develop a test input vector generation method. Also, test speed of our method for ICs fabricated with the state-of-art technology should be examined.

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