Static and Dynamic Behavior of Memory Cell Array Opens and Shorts in Embedded DRAMs

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Abstract: *Fault analysis of memory devices using defect injection and simulation is becoming increasingly important as the complexity of memory faulty behavior increases. In this paper, this approach is used to study the effects of opens and shorts on the faulty behavior of embedded DRAM (eDRAM) devices produced by Infineon Technologies. The analysis shows the existence of previously defined memory fault models, and establishes new ones. The paper also investigates the concept of dynamic faulty behavior and establishes its importance for memory devices. Conditions to test the newly established fault models are also given.*

Key words: *Embedded DRAM, functional fault models, fault primitives, defect simulation, opens, shorts.*

1 Introduction

The continued increase in the integration density of ICs has made it possible to use on-chip dynamic RAM cores, referred to as *Embedded DRAMs (eDRAMs)*, along with other electrical components. On the one hand, *e*DRAMs have many advantages over commodity DRAMs, such as an increased bandwidth, reduced power consumption, suitable memory organization and low electromagnetic interference [Iyer99]. On the other hand, *e*DRAMs create a number of new test challenges as a result of the nonstandard memory manufacturing techniques used, the limited external control on the internal behavior, and the limited number of parts manufactured as compared with commodity DRAMs.

To face these challenges, the faulty behavior of specific memory designs should be analyzed using robust fault modeling techniques that precisely describe the observed faulty behavior. Much of the work on functional fault modeling has been concerned with modeling faults sensitized by a *single* performed operation, which are referred to as *static FFMs* [vdGoor98, Adams96]. In this paper, it is shown that a large number of FFMs exist that have to be sensitized by a sequence of two or more operations, referred to as *dynamic FFMs*, that are especially important for DRAMs.

This paper establishes all static and a number of 2-operation dynamic FFMs in the memory cell array of an *e*DRAM, by injecting electrical open and short defects into the electrical model of an *e*DRAM. The impact of bridge defects on the behavior of the *e*DRAM memory cell array has already been analyzed [Al-Ars00]. Naik[93] has used this approach for static FFMs in SRAMs, while Nagi[96] has applied it to more general electrical devices.

This paper is organized as follows. Section 2 describes the used *e*DRAM simulation model, then Section 3 defines the static and dynamic FFMs targeted in this paper. In Section 4, the defects to be injected into the simulation model are defined and classified. Section 5 gives the methodology to be used for performing the simulations and extracting the FFMs. Section 6 discusses the simulation results, and Section 7 uses these results to derive detection conditions and extend current functional tests to detect the dynamic faulty behavior. Finally, Section 8 ends with the conclusions.

2 *e*DRAM simulation model

This section introduces the *e*DRAM simulation model used in the fault analysis. The simulation model is based on a design-validation model of an actual *e*DRAM produced by Infineon Technologies. A general description of this *e*DRAM and its test concept can be found in the literature [McConnell98]. Since the time needed for simulating a complete memory device is excessively long, the simulation model is simplified, taking two factors into consideration in order to preserve the model accuracy. First, removed components should be electrically compensated, and second, the resulting simplified circuit should describe enough of the memory to enable injecting the defects of interest.

Figure 1 shows a block diagram of the cell array column of the simulated *e*DRAM. (The blocks labeled OB1s,

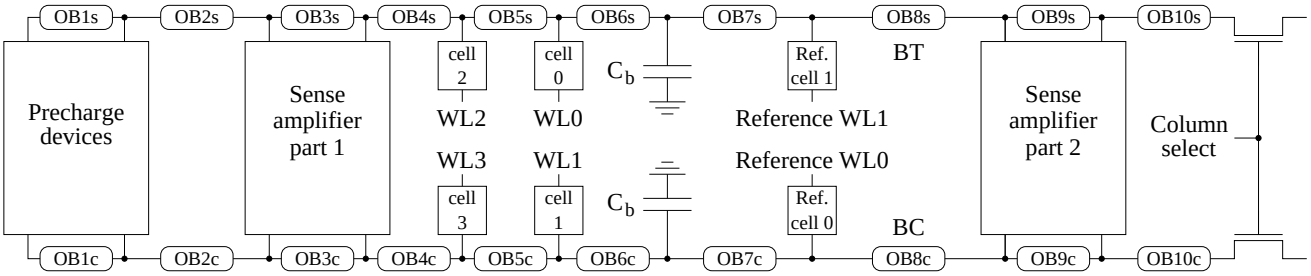

Figure 1. Cell array column of the *e*DRAM, where the possible locations of opens on BT and BC are indicated.

OB1c, OB2s, etc., are locations of opens on bit lines as discussed in Section 4.2. In a defect free model, these blocks represent no resistance on the bit lines.) This simplified simulation model contains a 2×2 cell array, in addition to two reference cells, precharge circuits and a sense amplifier. The removed memory cells are compensated by resistances and capacitances along the bit line. In addition to the shown cell array column, the simulation model contains one data output buffer needed to examine data on output lines, and a write driver needed to perform write operations. Although the general structure of the *e*DRAM model above is similar to that of a commodity DRAM, the used device parameters are modeled based on an *e*DRAM fabrication process. Therefore, the fault analysis results derived from this model may not precisely apply for other types of DRAM.

At the beginning of each simulation round, all capacitor voltages are properly initialized while the data output buffer is forced to contain a logic 1 at the true side. Since the assumption of proper voltage initialization is only valid for non-defective circuits, simulations are performed as the voltage level of defective nodes is modified as discussed in Section 5.

3 Definition of FFMs

In this section, the FFMs used in this paper are defined. First, a classification of the FFMs is presented with which the total space of faults can be divided into a number of classes. Then, four of these classes are discussed and used to define the targeted FFMs.

3.1 Classification of fault models

Two basic ingredients are needed to define any fault model: a list of performed memory operations and a list of corresponding deviations in the observed behavior from the expected one. The only functional deviations considered relevant to the faulty behavior are the stored logic value in the cell and the output value of a read operation.

Any difference between the observed and expected memory behavior can be denoted by the following notation $<S/F/R>$, referred to as a *fault primitive (FP)*. S describes the *sensitizing operation sequence (SOS)* that sensitizes the fault; F describes the value of the faulty cell, $F \in \{0,1\}$; and R describes the logic output level of a read operation, $R \in \{0,1,-\}$. The '–' is used in case a write, and not a read, is the operation that sensitizes the fault.

FPs can be classified according to $\#C$, the number of different cells accessed during an SOS, and according to $\#O$, the number of different operations performed in an SOS. A taxonomy of FPs is shown in Figure 2. A general treatment of possible SOS's performed on DRAMs has been done by vdGoor[00]. In this paper, we are only interested in SOS's performed on one memory cell, because we assume that fault effects of opens and shorts are localized to a single cell.

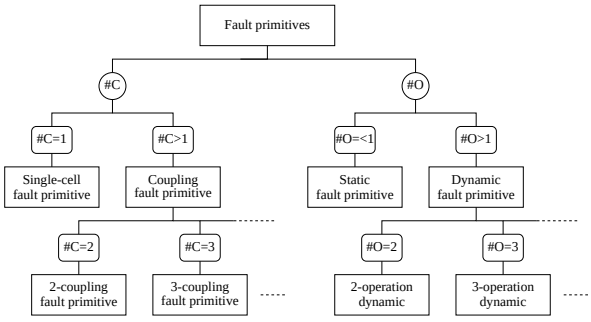

Figure 2. Taxonomy of fault primitives.

The notion of FPs makes it possible to give a precise definition of an FFM as understood for memory devices. This definition is presented next.

> A **functional fault model** (FFM) is a non-empty set of fault primitives (FPs).

3.2 Single-cell static FFMs

Single-cell static FFMs describe faults sensitized by performing at most one operation on the faulty cell. As men-

Table 1. All possible combinations of the values in the $<S/F/R>$ notation resulting in single-cell static FPs.

#	S	F	R	FP	Fault model
1	0	1	–	$<0/1/->$	SF_0
2	1	0	–	$<1/0/->$	SF_1
3	$0w0$	1	–	$<0w0/1/->$	WDF_0
4	$0w1$	0	–	$<0w1/0/->$	TF↑
5	$1w0$	1	–	$<1w0/1/->$	TF↓
6	$1w1$	0	–	$<1w1/0/->$	WDF_1
7	$0r0$	0	1	$<0r0/0/1>$	IRF_0
8	$0r0$	1	0	$<0r0/1/0>$	$DRDF_0$
9	$0r0$	1	1	$<0r0/1/1>$	RDF_0
10	$1r1$	0	0	$<1r1/0/0>$	RDF_1
11	$1r1$	0	1	$<1r1/0/1>$	$DRDF_1$
12	$1r1$	1	0	$<1r1/1/0>$	IRF_1

tioned earlier, a particular FP is denoted by $<S/F/R>$. S describes the value or operation that sensitizes the fault, $S \in \{0, 1, 0w0, 0w1, 1w0, 1w1, 0r0, 1r1\}$ for static FPs. F and R have already been defined in Section 3.1.

Now that the possible values for S, F and R are known for single-cell static FPs, it is possible to list all detectable FPs using this notation. Table 1 lists all 12 possible combinations of the values, in the $<S/F/R>$ notation, that result in FPs. The column 'Fault model' states the FFM defined by the corresponding FP.

All FPs listed in Table 1 are targeted in this paper. Below, they are used to define 6 different FFMs described in terms of non-empty sets of FPs.

1. **State faults (SF_x)**—A cell is said to have an SF if the logic value of the cell flips before it is accessed, even if no operation is performed on it[1]. Two types of SF exist: $SF_0 = \{<0/1/->\}$, with FP #1, and $SF_1 = \{<1/0/->\}$, with FP #2.

2. **Transition faults (TFx)**—A cell is said to have a TF if it fails to undergo a transition ($0 \rightarrow 1$ or $1 \rightarrow 0$) when it is written. Two types of TF exist: TF↑= $\{<0w1/0/->\}$, with FP #4, and TF↓= $\{<1w0/1/->\}$, with FP #5.

3. **Read disturb faults (RDF_x)** [Adams96]—A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns an incorrect value on the output. Two types of RDF exist: $RDF_0 = \{<0r0/1/1>\}$, with FP #9, and $RDF_1 = \{<1r1/0/0>\}$, with FP #10.

4. **Write disturb faults (WDF_x)**—A cell is said to have a WDF if a non-transition write operation ($0w0$ or $1w1$) causes a transition in the cell. Two types of WDF exist: $WDF_0 = \{<0w0/1/->\}$, with FP #3, and $WDF_1 = \{<1w1/0/->\}$, with FP #6.

5. **Incorrect read faults (IRF_x)**—A cell is said to have an IRF if a read operation performed on the cell returns the incorrect logic value, while keeping the correct stored value in the cell. Two types of IRF exist: $IRF_0 = \{<0r0/0/1>\}$, with FP #7, and $IRF_1 = \{<1r1/1/0>\}$, with FP #12.

6. **Deceptive read disturb faults ($DRDF_x$)** [Adams96]—A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, while it results in changing the contents of the cell. Two types of DRDF exist: $DRDF_0 = \{<0r0/1/0>\}$, with FP #8, and $DRDF_1 = \{<1r1/0/1>\}$, with FP #11.

The 6 FFMs defined above cover the space of all 12 single-cell static FPs of Table 1. Any single-cell static FFM can be represented as the union set of two or more of these 12 FPs. For example, if a defect results in a faulty behavior represented by an incorrect read-1 fault (IRF_1) and a read-0 disturb fault (RDF_0), then the corresponding behavior is described as $\{<1r1/1/0>\} \cup \{<0r0/1/1>\} = IRF_1 \cup RDF_0$.

3.3 Single-cell dynamic FFMs

FFMs sensitized by performing more than one operation on the faulty memory cell are called *dynamic fault models*. There are 2-operation, 3-operation, ..., dynamic fault models, depending on $\#O$. Here, we restrict ourselves to the analysis of 2-operation dynamic FFMs.

There are 30 different single-cell 2-operation dynamic FPs possible, but in order to reduce simulation time, not all 30 FPs are considered. We choose only to target the 4 dynamic SOS's $0w0r0$, $0w1r1$, $1w0r0$ and $1w1r1$ (in short $xwyry$), because in memory devices, an isolated write operation may not be sufficient to detect a fault since, externally, a cell needs to be read to detect the stored value set during the write.

The 4 targeted SOS's are capable of sensitizing 12 single-cell 2-operation FPs, which are used to define the following 3 FFMs. The names of these FFMs are chosen in such a way that they represent an extension of the single-cell static FFMs defined in Section 3.2.

[1]It should be noted that the state fault should be understood in the static sense. That is, the cell should flip in the short time period after initialization and before accessing the cell.

1. **Dynamic read disturb fault (RDF$_{xy}$)** is a fault whereby an $xwyry$ SOS changes the stored logic value to $\overline{y}$ and gives an incorrect output. Four types of dynamic RDF exist: RDF$_{00}$ = $\{<0w0r0/1/1>\}$, RDF$_{11}$ = $\{<1w1r1/0/0>\}$, RDF$_{01}$ = $\{<0w1r1/0/0>\}$, and RDF$_{10}$ = $\{<1w0r0/1/1>\}$.

2. **Dynamic incorrect read fault (IRF$_{xy}$)** is a fault whereby an $xwyry$ SOS returns the logic value $\overline{y}$ while keeping the correct state of the cell. Four types of dynamic IRF exist: IRF$_{00}$ = $\{<0w0r0/0/1>\}$, IRF$_{11}$ = $\{<1w1r1/1/0>\}$, IRF$_{01}$ = $\{<0w1r1/1/0>\}$, and IRF$_{10}$ = $\{<1w0r0/0/1>\}$.

3. **Dynamic deceptive read disturb fault (DRDF$_{xy}$)** is a fault whereby an $xwyry$ SOS returns the correct logic value y while destroying the state of the cell. Four types of dynamic DRDF exist: DRDF$_{00}$ = $\{<0w0r0/1/0>\}$, DRDF$_{11}$ = $\{<1w1r1/0/1>\}$, DRDF$_{01}$ = $\{<0w1r1/0/1>\}$, and DRDF$_{10}$ = $\{<1w0r0/1/0>\}$.

4 Simulated defects

In this section we discuss the defects to be injected in the *e*DRAM model.

4.1 Classification of defects

The defects to be considered for injection and analysis are modeled at the electrical level by parasitic components with a given impedance. The impedance (Z) consists of a resistance (R) and a capacitance (C) connected in parallel between two defective nodes. Depending on the defective nodes the injected defects are connected to, the defects may be classified into opens, shorts and bridges. The effect of bridges has been addressed in an earlier paper [Al-Ars00].

Opens represent unwanted impedances on a signal line that is supposed to conduct perfectly, while shorts represent unwanted impedances between a signal line and V_{DD} or GND. For an open defect, the impedance value is given by Z_{op} and is predominantly resistive (i.e., $C_{op} \approx 0$ making $Z_{op} \approx R_{op}$). The open resistance may take any value in the resistance domain, which gives $0 \leq Z_{op} \leq \infty\ \Omega$. The fact that opens result in negligible capacitive coupling between the broken nodes has been substantiated by Henderson[91]. For a short, the impedance value is denoted by Z_{sh} and may have resistive and capacitive components. The value of R_{sh} for a short may again have any value ($0 \leq R_{sh} \leq \infty\ \Omega$), while C_{sh} is bounded by some given realistic limits ($C_{min} < C_{sh} < C_{max}$). The lower bound of the short capacitance is taken to be 0 F ($C_{min} = 0$ F), while the maximum bound is considered to be equal to the bit line capacitance in the memory ($C_{max} = C_b$). The reason behind this choice is that the bit line has the highest capacitance along a single cell array column. Therefore, it is highly unexpected for a parasitic capacitance to have yet a higher value.

Table 2. Single-cell FFMs and complementary FFMs.

Fault model	Complementary	Fault model	Complementary
SF$_0$	SF$_1$	IRF$_{00}$	IRF$_{11}$
IRF$_0$	IRF$_1$	DRDF$_{00}$	DRDF$_{11}$
DRDF$_0$	DRDF$_1$	RDF$_{00}$	RDF$_{11}$
RDF$_0$	RDF$_1$	IRF$_{01}$	IRF$_{10}$
WDF$_0$	WDF$_1$	DRDF$_{01}$	DRDF$_{10}$
TF↑	TF↓	RDF$_{01}$	RDF$_{10}$

By analyzing the electrical circuits of the cell array column, we notice some symmetry in the topology of these circuits. This results in a symmetry in the faulty behavior, which can be used to reduce the number of defects to be simulated and analyzed. A defect D1 at a given position shows the **complementary faulty behavior** to a defect D2 at another position, if the faulty behavior of D1 is the same as that of D2, with the only difference that all 1s are replaced by 0s, and vice versa. Table 2 lists the single-cell FFMs defined in Section 3 and their complementary counterparts.

4.2 Locations of opens

The locations of opens within memory cells (OC), along bit lines (OB) and on word lines (OW) are enumerated and provided with a label for future reference. All possible different opens are taken into consideration which eliminates the need to use layout information.

Opens within a memory cell (OC) can occur at any node within the storage cell. Figure 3(a) shows one memory cell where the three possible defect locations are indicated. The choice has been made to simulate the opens within a cell on the true bit line (BT), and these defects are therefore labeled as OCxs ('s' for simulated, see Table 3). Consequently, the faulty behavior of an open in a cell on the complement bit line (BC), which is labeled as OCxc ('c' for complementary), may be derived from the corresponding simulated one because it shows the complementary faulty behavior.

Opens along a bit line (OB) can occur anywhere on the bit line. Figure 1 shows a complete cell array column with BT and BC together with the bit line opens. The bit lines

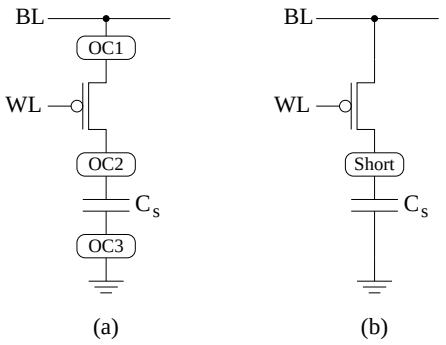

Figure 3. One *e*DRAM cell with possible locations of (a) opens and (b) shorts.

Table 3. Simulated and complementary opens within a cell.

OC on BT	OC on BC	Description
OC1s	OC1c	Pass transistor connection to bit line broken
OC2s	OC2c	Pass transistor connection to storage capacitor broken
OC3s	OC3c	Cell connection to ground broken

are divided into 10 regions, each of which may contain an open. Every open on BT has its complementary open on BC and vice versa. Thus, only opens present on BT are simulated. Every defect on BT is given the name OBxs, while its counterpart on BC is given the name OBxc.

Opens on a word line (OW) can only be at one position between the row decoder and the gate of the pass transistor of a memory cell. The behavior of the cell with an open on its word line is the same for every cell on BT and complementary to that on BC. Therefore, only one open is simulated, namely that on WL0, which is called OW1s. The open located on WL1 is called OW1c.

4.3 Locations of shorts

The possible locations of shorts within memory cells (SC) and along bit lines (SB) are enumerated and provided with a label for future reference. All possible shorts are analyzed with the exception of: 1) shorts between V_{DD} and ground since they are power shorts, and 2) gate oxide shorts (GOS's) since they are layout defects that are modeled at the electrical level as bridges [Al-Ars00].

Shorts within a memory cell (SC) can be injected within the storage cell at only one node between the pass transistor and the storage capacitor, as shown in Figure 3(b). This gives two possible shorts, SC1 which is a connection between the cell and V_{DD}, and SC2 which is a connection between the cell and GND. Every short in a cell on BT has its complementary short in a cell on BC and vice versa. Thus, only shorts in cells on BT are simulated. Shorts in cells on BT are called SCxs, while their counterparts on BC are called SCxc.

Shorts along a bit line (SB) can connect each of BT and BC to either V_{DD} or GND. A bit line short to V_{DD} is called SB1, while a bit line short to GND is called SB2. Every short on BT has its complementary short on BC and vice versa. Thus, only shorts along BT are simulated. Shorts on BT are called SBxs, while their counterparts on BC are called SBxc.

5 Simulation methodology

This section discusses the simulation performed for opens and shorts. The simulator used is called Pstar, which is a spice based analog simulator used by Philips.

5.1 Simulation of opens

The behavior of the *e*DRAM is studied after injecting and simulating each of the opens defined in Section 4.2. The analysis considers open resistances within the range ($10 \leq R_{op} \leq 10$ MΩ) on a logarithmic scale using 5 points per decade, in addition to $R_{op} = \infty\ \Omega$. Each injected open in the memory model creates floating nodes, the voltage of which is varied between V_{DD} and GND on a linear scale using 10 points. When an interesting faulty behavior is observed, more detailed simulations are performed. Determining the floating node resulting from each injected open depends on the type of the open. For opens along bit lines, the floating node is always taken to be the one connected to column access devices, not the one connected to the precharge devices since this node is precharged to a known voltage at the beginning of each operation. The floating node for opens within memory cells is taken to be the node connected to the cell capacitor. For opens on word lines the floating node is the node connected to the memory cell.

For each value of the open resistance (R_{op}) and of the initial floating node voltage (U_{init}), all the SOS's associated with the targeted FPs defined in Section 3 are performed and inspected for proper functionality. As a result, the faulty behavior resulting from the analysis of opens is represented as regions in the (U_{init}, R_{op}) plane. Each region contains a number of sensitized FPs that describe the FFM of the memory in this region.

As an example, the results of the fault analysis performed on OC1s (see Figure 3(a)) are given in Figure 4, which shows the observed faulty behavior in the

(U_{init}, R_{op}) plane. In the figure, TFd stands for TF↓, TFu stands for TF↑, while V_{mp} is the mid-point voltage (the threshold voltage between logic 0 and logic 1). The figure shows a number of different fault regions for different combinations of U_{init} and R_{op}. The fault regions may be classified according to the initial floating node voltage under which they can be detected as follows:

A. Faults detectable with $U_{init} = V_{DD}$

   A1. Fault region TF↓ ∪ RDF_{10}

   A2. Fault region RDF_{10}

B. Faults detectable with U_{init} = GND

   B1. Fault region $IRF_0 \cup TF\uparrow \cup IRF_{00} \cup DRDF_{01}$

   B2. Fault region $IRF_0 \cup TF\uparrow \cup IRF_{00}$

   B3. Fault region $IRF_0 \cup TF\uparrow \cup RDF_{00}$

   B4. Fault region $RDF_0 \cup RDF_{00}$

   B5. Fault region TF↑

C. Faults only detectable with GND $< U_{init} < V_{DD}$

   C1. Fault region $RDF_0 \cup WDF_0 \cup RDF_{00}$

   C2. Fault region RDF_0

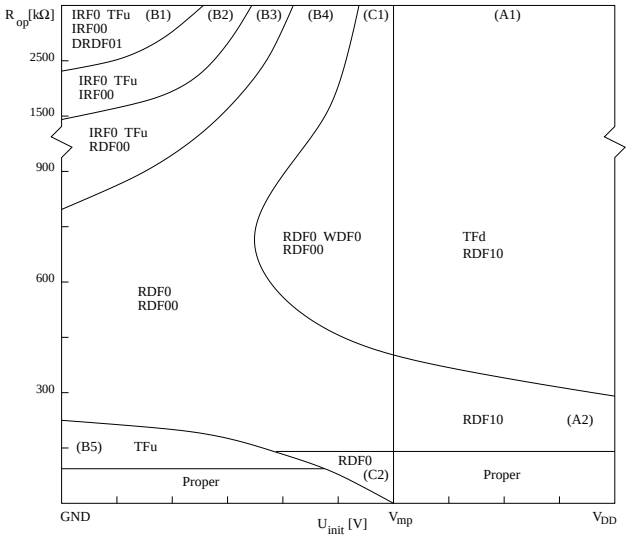

Figure 4. Summary of the fault analysis results of the defect OC1s in the (U_{init}, R_{op}) plane under $T = 27°$ C.

Inspecting the faulty behavior shown in the figure reveals that there are two fault regions C1 and C2 not detectable at a U_{init} equal to either V_{DD} or GND. Moreover, the fault region C1 contains the FFM WDF_0 which cannot be detected in any other fault region. This indicates that performing the fault analysis with all possible U_{init} values is important if all the sensitized FFMs resulting from a given defect are to be established.

The fault region A2 only contains the FFM RDF_{10}, which means that $1w0r0$ is the only failing SOS in this region. This, in turn, means that performing the traditional *static* analysis on this fault region reveals no improper memory behavior. Only by applying *dynamic* SOS is it possible to detect this improper behavior. This shows the significance of performing the dynamic analysis on memory devices.

5.2 Simulation of shorts

The behavior of the *e*DRAM is studied after injecting and simulating each of the shorts defined in Section 4.3. The short impedance can have a resistive and a capacitive component. The short resistor and short capacitor are connected in parallel between the defective node and the power supply. The short resistance (R_{sh}) is varied in the same way as R_{op}, while the short capacitance (C_{sh}) is varied between 0 F and C_b on a linear scale using 10 points.

For each value of R_{sh} and C_{sh}, all the SOS's associated with the *targeted* FPs defined in Section 3 are performed and inspected for proper functionality. As a result, the faulty behavior resulting from the analysis of shorts is represented as regions in the (C_{sh}, R_{sh}) plain.

As an example, the results of the fault analysis performed on SC1s (short between memory cell and V_{DD}) are shown in Figure 5, where TFd stands for TF↓. According to the figure, the faulty behavior of SC1s depends more on R_{sh} than it depends on C_{sh}. There are two fault regions shown in the figure, listed next with increasing R_{sh} value.

1. Fault region $SF_0 \cup RDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10}$

2. Fault region $RDF_0 \cup WDF_0 \cup TF\downarrow \cup RDF_{00} \cup RDF_{10}$

The figure shows a relatively simple faulty behavior of the short defect SC1s as compared with that of the open defect OC1s of Figure 4. As the short resistance increases, the number of faulty SOS's decreases until the memory starts to function properly with $R_{sh} > 400$ kΩ when $C_{sh} = 0$ F. On the other hand, the faulty behavior is, to a large extent, independent of the value of the short capacitance. Nevertheless, as the defect capacitance increases, the regions of faulty behavior decrease slightly in size, while the size of the region of proper operation increases. Generally, the faulty behavior resulting from a short remains almost the same as long as C_{sh} remains less than the storage capacitance of the memory cell C_s.

6 Simulation results

All opens and shorts defined in Section 4 have been injected, simulated and analyzed. The analysis results

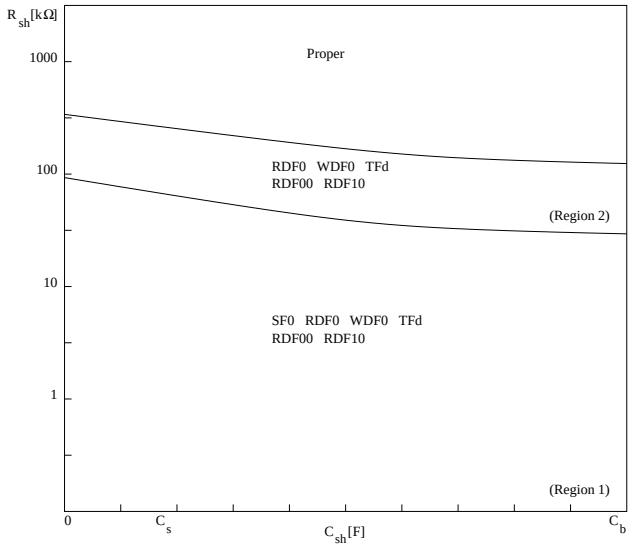

Figure 5. Summary of the fault analysis results for the SC1s short to V_{DD} in the (C_{sh}, R_{sh}) plane under $T = 27°$ C.

of opens are organized in figures depicting parts of the (U_{init}, R_{op}) plane, while the analysis results of shorts are organized in figures depicting a part of the (C_{sh}, R_{sh}) plane [Al-Ars99]. In the following, the results of opens are discussed first, then the results of shorts.

6.1 Results of opens

Table 4 gives a summary of the detected FFMs for each open defect within memory cells, along bit lines and on word lines. The first column in the table specifies the analyzed defects (in case a number of defects sensitize the same FFMs they are listed together), while the second and third columns list the FFMs detected for the simulated and complementary instances of these defects, respectively. Inspecting the table reveals that all FFMs defined in Section 3 are present and result from at least one defect.

The table shows that all opens within cells cause the same faulty behavior, while the behavior caused by opens on bit lines changes significantly by changing the position of the open. Moreover, some opens can cause a faulty behavior more easily than others (i.e., with less open resistance). The most sensitive position for an open is that at OB7, where an open with an open resistance as low as 200 Ω can result in a faulty memory behavior. The table shows that all defects cause static FFMs, and that most opens result in 2-operation dynamic FFMs (with the exception of OB1, OB2 and OB3).

It is important from a testing point of view to state the detected fault regions that only show dynamic faulty behavior, since for these regions testing for static faulty behavior cannot detect the defect. Table 5 lists all strictly dynamic fault regions detected in the analysis. The first column states the open resulting in the fault region, the second column describes the faulty behavior of the dynamic fault region, and the third column gives information about the fault region in the (U_{init}, R_{op}) plane. According to the table, there are four 2-operation FFMs that appear in fault regions with strictly dynamic behavior; they are the four types of the dynamic read disturb fault (RDF_{xy}).

Table 4. Summary of the observed FFMs for each open.

Open	Simulated	Complementary
OC1–3	TF↑, TF↓, WDF_0, RDF_0, IRF_0, RDF_{00}, RDF_{01}, RDF_{10}, IRF_{00}, DRDF_{01}	TF↓, TF↑, WDF_1, RDF_1, IRF_1, RDF_{11}, RDF_{10}, RDF_{01}, IRF_{11}, DRDF_{10}
OB1–3	RDF_1	RDF_0
OB4–5	TF↑, WDF_1, RDF_1, DRDF_1, RDF_{01}, RDF_{11}	TF↓, WDF_0, RDF_0, DRDF_0, RDF_{10}, RDF_{00}
OB6	TF↓, WDF_0, RDF_0, RDF_1, IRF_1, RDF_{01}, RDF_{11}, IRF_{01}, IRF_{11}, DRDF_{00}, DRDF_{10}	TF↑, WDF_1, RDF_1, RDF_0, IRF_0, RDF_{10}, RDF_{00}, IRF_{10}, IRF_{00}, DRDF_{11}, DRDF_{01}
OB7–8	TF↓, WDF_0, RDF_1, IRF_1, DRDF_0, RDF_{01}, RDF_{11}, IRF_{01}, IRF_{11}, DRDF_{00}, DRDF_{10}	TF↑, WDF_1, RDF_0, IRF_0, DRDF_1, RDF_{10}, RDF_{00}, IRF_{10}, IRF_{00}, DRDF_{11}, DRDF_{01}
OB9	RDF_0, IRF_0, DRDF_{00}, DRDF_{10}	RDF_1, IRF_1, DRDF_{11}, DRDF_{01}
OB10	TF↓, IRF_0, RDF_{10}, DRDF_{10}	TF↑, IRF_1, RDF_{01}, DRDF_{01}
OW1	SF_0, TF↑, TF↓, RDF_0, IRF_0, RDF_{00}, RDF_{10}, IRF_{00}, IRF_{10}	SF_1, TF↑, TF↓, RDF_1, IRF_1, RDF_{11}, RDF_{01}, IRF_{11}, IRF_{01}

Table 5. Strictly dynamic fault regions resulting from opens.

Open	Simulated	Complementary	Region
OC1–3	RDF_{10}	RDF_{01}	$150\ \mathrm{k\Omega} < R_{op} < 450\ \mathrm{k\Omega}$
OB4–5	RDF_{01}	RDF_{10}	$10\ \mathrm{k\Omega} < R_{op} < 20\ \mathrm{k\Omega}$
OB6	RDF_{01}	RDF_{10}	$25\ \mathrm{k\Omega} < R_{op} < 75\ \mathrm{k\Omega}$
	$\mathrm{RDF}_{01} \cup \mathrm{RDF}_{11}$	$\mathrm{RDF}_{10} \cup \mathrm{RDF}_{00}$	$75\ \mathrm{k\Omega} < R_{op} < 125\ \mathrm{k\Omega}$

6.2 Results of shorts

Table 6 gives a summary of the detected FFMs for each short defect within memory cells and along bit lines. The first column in the table lists the analyzed shorts, while the second and third columns list the FFMs detected for the simulated and complementary instances of these defects, respectively. Inspecting the table reveals that, contrary to opens, not all the FFMs defined in Section 3 result from short defects. The table shows that all shorts cause both static and 2-operation dynamic FFMs.

The only strictly dynamic fault region detected in the analysis of shorts is caused by SC2. The simulated faulty behavior of this region is $\mathrm{RDF}_{01} \cup \mathrm{RDF}_{11}$, while the complementary faulty behavior is $\mathrm{RDF}_{10} \cup \mathrm{RDF}_{00}$. This strictly dynamic region spreads across $300\ \mathrm{k\Omega} < R_{sh} < 1.2\ \mathrm{M\Omega}$ with a short capacitance of 0 F. Just like the case with opens, the FFMs present in this fault region are the four types of the dynamic read disturb fault (RDF_{xy}).

Table 6. Summary of the observed FFMs for each short.

Short	Simulated	Complementary
SC1	SF_0, $TF\downarrow$, WDF_0, RDF_0, RDF_{00}, RDF_{10}	SF_1, $TF\uparrow$, WDF_1, RDF_1, RDF_{11}, RDF_{01}
SC2	SF_1, $TF\uparrow$, WDF_1, RDF_1, RDF_{01}, RDF_{11}	SF_0, $TF\downarrow$, WDF_0, RDF_0, RDF_{10}, RDF_{11}
SB1	$TF\downarrow$, WDF_0, RDF_0, RDF_{00}, RDF_{10}	$TF\uparrow$, WDF_1, RDF_1, RDF_{11}, RDF_{01}
SB2	$TF\uparrow$, WDF_1, RDF_0, RDF_1, RDF_{00}, RDF_{01}, RDF_{10}, RDF_{11}	$TF\downarrow$, WDF_0, RDF_1, RDF_0, RDF_{11}, RDF_{10}, RDF_{01}, RDF_{00}

7 Test implications

The fault analysis performed on the cell array column of the *e*DRAM shows that all defined static and targeted dynamic FPs do occur. Moreover, some defects result in a faulty behavior with only dynamic fault models by performing certain SOS's on a memory cell. In order to ensure that a particular memory cell array is not faulty, tests should be developed to sensitize and detect all static and dynamic FFMs resulting from the sensitized FPs. Many tests have been proposed to detect static FFMs, such as MATS+, March C– [vdGoor98] and March LA [vdGoor97].

In order to construct a test that uncovers dynamic FFMs, it is important first to derive detection conditions for these FFMs. As shown in Tables 4 and 6, all targeted dynamic FFMs have been observed in our study. These dynamic FFMs are RDF_{xy}, IRF_{xy} and $DRDF_{xy}$, where x and $y \in \{0,1\}$. These dynamic FFMs can be detected by a given march test if it contains a march element with the following operation sequences:

1. $\Updownarrow (...0, w0, r0, r0, ...)$ for RDF_{00}, IRF_{00} & $DRDF_{00}$
2. $\Updownarrow (...0, w1, r1, r1, ...)$ for RDF_{01}, IRF_{01} & $DRDF_{01}$
3. $\Updownarrow (...1, w0, r0, r0, ...)$ for RDF_{10}, IRF_{10} & $DRDF_{10}$
4. $\Updownarrow (...1, w1, r1, r1, ...)$ for RDF_{11}, IRF_{11} & $DRDF_{11}$

where $(...0)$ and $(...1)$ specify the state of the cell before performing the first write operations. The first read operation in the conditions above sensitizes and detects dynamic RDF_{xy} and IRF_{xy}, while $DRDF_{xy}$ is sensitized by the first read operation and detected by the second.

The above detection conditions can be used to extend existing tests designed for static FFMs to detect 2-operation dynamic FFMs. As an example, March LA is a march test designed to detect some static FFMs. A number of operations can be added to the march elements of March LA based on the detection conditions to make it capable of detecting the observed dynamic FFMs. Figure 6(a) shows the conventional March LA test, while Figure 6(b) shows the extended version designed to detect the 2-operation dynamic FFMs [Al-Ars99]. The operations added to March LA are shown in the figure in bold face.

$$\{\Updownarrow(w0); \Uparrow(r0, w1, w0, w1, r1); \Uparrow(r1, w0, w1, w0, r0); \Downarrow(r0, w1, w0, w1, r1); \Downarrow(r1, w0, w1, w0, r0); \Downarrow(r0)\}$$

(a)

$$\{\Updownarrow(w0); \Uparrow(r0, w1, w0, w1, r1, \mathbf{r1}); \Uparrow(r1, w0, w1, w0, r0, \mathbf{r0}); \Downarrow(r0, w1, w0, w1, \mathbf{w1}, \mathbf{r1}, r1); \Downarrow(r1, w0, w1, w0, \mathbf{w0}, \mathbf{r0}, r0); \Downarrow(r0)\}$$

(b)

Figure 6. (a) Conventional March LA test. (b) Extended March LA version designed to detect the observed 2-operation dynamic FFMs.

8 Conclusions

In this paper, the faulty behavior of an *e*DRAM has been analyzed using open and short injection and circuit simulation. The fault analysis has not been restricted to the static memory behavior, but the 2-operation dynamic behavior has also been included. Known static FFMs have been observed and related to given opens or shorts in the memory. New static FFMs (SF_x and WDF_x) and a number of new dynamic FFMs (RDF_{xy}, IRF_{xy} and $DRDF_{xy}$) have been introduced and established. The analysis showed that dynamic faulty behavior can take place in the absence of static faulty behavior. Finally, the results of the analysis have been used to derive detection conditions for the observed dynamic FFMs.

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