A Design Strategy for Low-Voltage Low-Power Continuous-Time $\Sigma\Delta$ A/D Converters

Friedel Gerfers, Yiannos Manoli

Institute of Microelectronics
University of Saarland
D-66 123 Saarbruecken, Germany
E-mail: gerfers@ee.uni-sb.de, manoli@ee.uni-sb.de

Abstract

This paper presents a design strategy for low-voltage low-power $\Sigma\Delta$ analog-to-digital (A/D) converter using a continuous-time (CT) lowpass loopfilter. An improved method is used to find the optimal $\Sigma\Delta$ modulator implementation with respect to a minimal power consumption on the one hand and to fulfil a rapid prototyping approach on the other hand. The influence of the low supply voltage as well as circuit nonidealities on the overall $\Sigma\Delta$ modulator is determined and verified by behavioral simulations. Transistor-level simulation results of a $1.5\ V$ CT $\Sigma\Delta$ A/D converter show a 75 dB dynamic range in a bandwidth of $25kHz$.

1. Introduction

The rapid growing market of portable electronic systems such as wireless communication devices or battery powered medical devices increases the demand for developing low-voltage and low-power circuit techniques and building blocks. The main driving force for low-voltage CMOS design arises from the continuing trend towards deep submicron transistor dimensions. Reducing the power dissipation in integrated circuits is required to minimize the recharging cycles or extend the battery lifetime as much as possible. Furthermore, the increasing complexity on a chip results in an increase of power density and consequently the demand for power reduction.

An important building block of such systems is an analog-to-digital converter (ADC). Sigma-Delta ($\Sigma\Delta$) A/D converters are very attractive because they achieve high accuracy for narrow band signals with only a few critical analog components [9]. The use of CT loop filters provides several advantages over switched capacitor implementations. The required GBW of the integrators for a fixed sampling frequency (f_S) is approximately a factor of 3 lower compared to the discrete time counterparts. This results in further power savings or otherwise a CT A/D converter can operate at higher frequencies. CT loop filter realisations have an implicit anti-alias filter [8].
On the other hand CT $\Sigma\Delta$ converters are more sensitive to clock jitter [9] and extra loop delay [8].

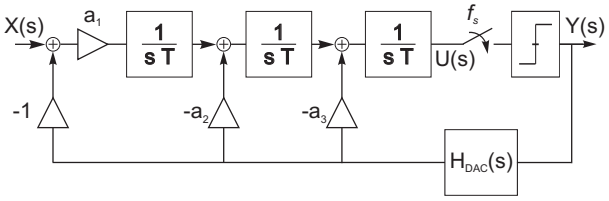

Figure 1. A general structure of a 3rd-order single-bit CT $\Sigma\Delta$ modulator. X(s) is bandlimited within f_B.

For low-voltage/low-power applications the single loop architecture as shown in Fig. 1 is the preferred structure over cascaded stages [5], because single loop topologies do not have stringent requirements (e.g. on the DC-gain) for the amplifiers except for the first stage.

In this paper, a design strategy for low-voltage/low-power continuous-time $\Sigma\Delta$ converters is proposed. This concept is based on the Figure of Merit (FOM) which takes the overall power consumption (P), the dynamic range (DR) and the signal bandwidth (f_B) into account to find the optimal $\Sigma\Delta$ converter implementation with respect to these design parameters (Sec. 2). This strategy considerably simplifies the design flow of low-voltage $\Sigma\Delta$ converters and makes it more systematic. In Section 3 the filter coefficients for this optimal A/D converter realization will be determined depending on the digital-to-analog converter (DAC) feedback impulse response. The influence of cir-

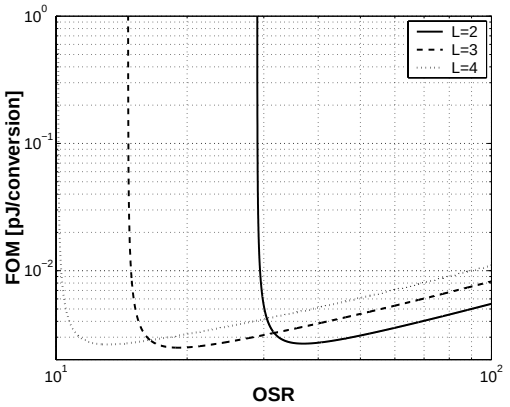

Figure 2. Estimated FOM as a function of the oversampling ratio OSR for different modulator orders (L).

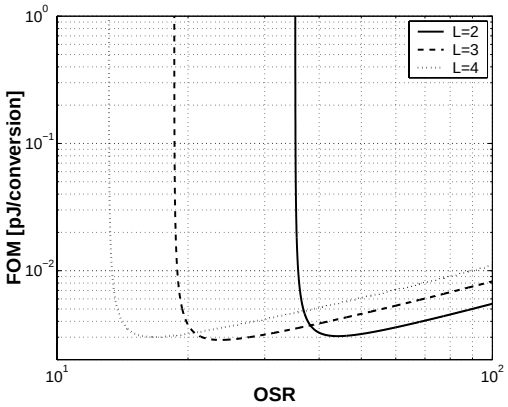

Figure 3. Estimated FOM as a function of the oversampling ratio OSR for different modulator orders and a maximum out-of-band gain of 1.5.

cuit nonidealities on the overall modulator performance is briefly reviewed in Sec. 4.

The next step of the design strategy is to specify the operation point of the transistors in the low-voltage building blocks, so that the effect of the low supply voltage on the total power consumption, noise contribution as well as on the input and output voltage swing will be considered.

Finally, the parameters that determine the signal-to-noise ratio (SNR) have to be evaluated (Sec. 6). Consequently, these parameters can be set so that the desired resolution can be achieved. The verification of the theoretical results will be done in Section 7 by behavioral and transistor-level simulations.

2. Powerefficient Modulator Implementation

As described above a single loop architecture was chosen. To find the optimal $\Sigma\Delta$ modulator implementation with respect to a minimal power consumption for a given oversampling ratio ($OSR = \frac{f_S}{2\,f_B}$) on the one hand and fulfil also a rapid prototyping approach on the other hand the Figure of Merit was used [2]. The estimations in Sec. 2 to Sec. 4 were done with the symbolic software tool MAPLE. The minimal FOM shows the optimal structure that fulfils the specifications (Fig. 2).

$$FOM = \frac{P}{DR \cdot 2f_B}. \tag{1}$$

The required resolution is $b = 10$ bit in a bandwidth of $25kHz$. The dynamic range (DR) calculations consider only quantization (N_Q) and thermal noise (N_{Th}):

$$N_Q = \frac{(2\hat{V})^2}{12}\frac{\pi^{2L}}{(2L+1)\,OSR^{2L+1}} \tag{2}$$

$$N_{Th} = \frac{kT}{OSR \cdot C} \tag{3}$$

where L is the modulator order and $\hat{V}$ is peak input voltage. The overall power consumption P is made up of a static and dynamic portion of the analog part (opamps and integrators) and a portion of the digital part (comparator, flip-flop and logic):

$$P \approx aIV_{DD}L + 2L(2\hat{V})^2 C f_s + 10QP_{inv}(1ns)f_s \tag{4}$$

where a describe the number of current branches and $I = \frac{g_m^2}{2\beta}$. The required transconductance g_m is given by the GBW and required capacitance C. Q represents the size of the digital part converted in CMOS gate-equivalents inverters with a power consumption of $50nW/MHz$. With Equations (2) to (5) one can calculate the required capacitance C:

$$C = \frac{kT}{OSR}\left(\frac{\frac{\hat{V}^2}{2}}{3 \cdot 2^{2b-1}} - N_Q\right)^{-1} \tag{5}$$

The best FOM is obtained with a third order modulator with an OSR close to 18.

A more realistic FOM estimation takes also the scaling of the noise transfer function (NTF) into account. This is necessary, since high-order modulators with $L > 2$ are unstable. For the FOM computation a rule-of-thumb with an out-of-band gain ($\hat{H}_\infty = 2^L$) of 1.5 was used. This results to Figure 3.

The minimal FOM as well as the minimal OSR at which the desired performance is achieved is increased. In other words, the minimal power consumption increases for a fixed resolution and signal bandwidth. Again, the best

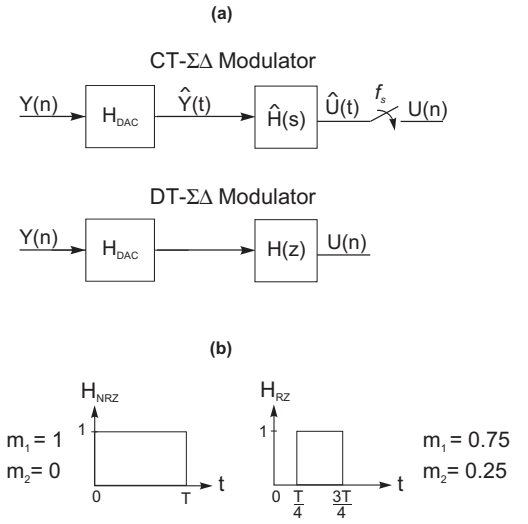

Figure 4. a) Open-loop CT $\Sigma\Delta$ modulator and the DT equivalent. b) NRZ pulse (delay t_d = 0, pulse width τ = T) and RZ ($t_d = 1/4T$, $\tau = 1/2T$) DAC feedback impulse responses.

FOM is obtained with a third order modulator with an OSR of approximately 23. Taking also parasitic capacitances and additional noise and distortion into account a higher OSR is required. Based on these criteria a third order CT single loop modulator with an $OSR = 32/48$ was implemented. Now, the overall modulator architecture is dedicated. The next step is to determined the CT loop filter.

3. DT/CT Modulator Equivalence

The overall behavior of a CT $\Sigma\Delta$ modulator loop is nonetheless discrete time due to the fact that the loop is sampled in time by the clocked quantizer (Fig. 1). Based on this fact the CT open-loop filter $\hat{H}(s)$ can be replaced by a DT equivalent $H(z)$ (Fig. 4a) with respect to the DAC feedback impulse response. Fig. 4b shows a non-return-to-zero (NRZ) and return-to-zero (RZ) DAC impulse response. Thus design and simulation of the ideal CT $\Sigma\Delta$ modulator can be done in discrete time domain [8] [3].

The coefficients a_i of the continuous-time modulator can be calculated as a function of the DT integrator coefficients b_i by using the modified Z-transform [6]. The loop filter for the CT third-order modulator results in:

$$\begin{aligned} \mathcal{Z}(\hat{H}(s)) &= \mathcal{Z}_{m1}\left(\frac{-a_1}{Ts^2}+\frac{-a_2}{T^2s^3}+\frac{-a_3}{T^3s^4}\right) \\ &- \mathcal{Z}_{m2}\left(\frac{-a_1}{Ts^2}+\frac{-a_2}{T^2s^3}+\frac{-a_3}{T^3s^4}\right) \end{aligned} \quad (6)$$

with $m_1 = 1 - \frac{t_d}{T}$ and $m_2 = 1 - \frac{t_d}{T} - \frac{\tau}{T}$ where t_d is the DAC delay and tau the DAC pulse width. Using Tab. 1 and the NRZ-DAC feedback scheme ($m_1 = 1,\ m_2 = 0$) respectively the RZ-DAC feedback scheme ($m_1 = 3/4,\ m_2 = 1/4$), the coefficients a_i are:

$$\begin{aligned} a_{1_{NRZ}} &= b_1b_2b_3 & a_{1_{RZ}} &= 2b_1b_2b_3 \\ a_{2_{NRZ}} &= b_1b_2b_3 + b_2b_3 & a_{2_{RZ}} &= 2b_1b_2b_3 + 2b_2b_3 \\ a_{3_{NRZ}} &= \frac{b_1b_2b_3}{3} + \frac{b_2b_3}{2} + b_3 & a_{3_{RZ}} &= \frac{35}{48}b_1b_2b_3 + b_2b_3 + 2b_3 \end{aligned} \quad (7)$$

$Z_m(1/s^2)$	$\frac{mT}{z-1} + \frac{T}{(z-1)^2}$
$Z_m(1/s^3)$	$\frac{T^2}{2}[\frac{m^2}{z-1} + \frac{2m+1}{(z-1)^2} + \frac{2}{(z-1)^3}]$
$Z_m(1/s^4)$	$\frac{T^3}{6}[\frac{m^3}{z-1} + \frac{3m^2+3m+1}{(z-1)^2} + \frac{6m+6}{(z-1)^3} + \frac{6}{(z-1)^4}]$

Table 1. Modified Z-transform

4. Influence of Circuit Nonidealities

In this section, the influence of a number of circuit nonidealities is analytical determined using MAPLE in order to minimize their effect on the entire modulator performance. The corresponding behavioral simulation results are shown in Sec. 7.1.

The power dissipation of the first integrator is the major contributor to the overall power dissipation in $\Sigma\Delta$ modulators, therefore a substantial amount of power can be saved by a proper circuit design. On the other hand the nonidealities in the input transconductor (distortion and noise) and the first integrator (finite DC-gain, distortion and noise) reduce the performance of the entire A/D converter since these errors add directly to the input signal.

4.1. Leaky CT Integrator

In presence of a finite amplifier gain one can express the inband noise power (IBN) at the output of the third order single-bit modulator as follows [1]:

$$IBN \approx \frac{\Delta^2}{12} \cdot \frac{\pi^6}{7a_1^2}\left[\frac{1}{OSR^7} + \frac{21}{5OSRA_V^2}\right] \quad (8)$$

The effect is shown in Fig. 5. In order to minimize the additional noise caused by integrator leakage one can compute the critical DC-gain value A_V where the excess parasitic noise degrades the signal-to-noise ratio by 3 dB. For the 3rd-order modulator this critical gain is equal to:

$$A_{V,3dB} \approx \sqrt{\frac{21}{5}} \cdot \frac{OSR}{\pi} \approx 21. \quad (9)$$

[1] The nonlinear quantizer is modelled by a white-noise source.

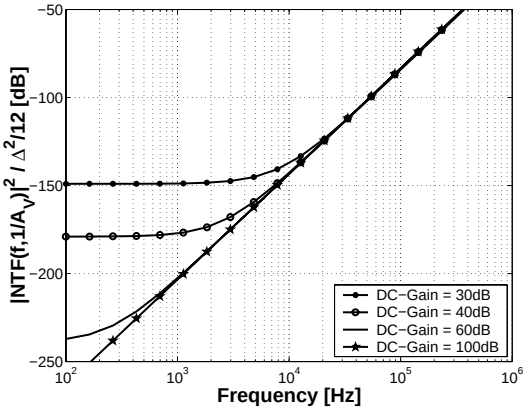

Figure 5. The rms quantization noise of a 3rd-order modulator for various DC-gains.

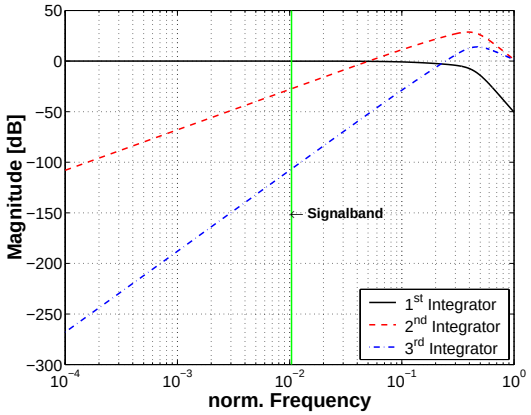

Figure 6. Transfer functions of circuit errors resulting from the three integrators

Eq. (9) shows the minimum gain if only leakage is considered [1]. Taking also distortion into account the required transconductance and bias current of the input transistors have to be much higher (Sec. 4.4).

4.2. Non-dominant Integrator Poles

Non-dominant integrator poles degrade the loop stability of the entire modulator by pushing the modulator poles closer to the imaginary axis. Taking only the dominant pole (p_{dom}) of the amplifier into account one can express the in-band noise at the output of the third order modulator as follows:

$$IBN \approx \frac{\Delta^2}{12} \cdot \frac{\pi^6}{7a_1^2 OSR^7} \cdot [1 + \frac{1}{2\pi c}]^6 \quad (10)$$

$$c = GBW/2\pi fs \quad \text{and} \quad GBW \approx A_V \cdot p_{dom} \quad (11)$$

To limit the additional noise due to the non-dominant integrator pole to 3dB the minimal ratio of the amplifier gain-bandwidth (GBW) to the sampling frequency f_s is shown in Eq. 12.

$$c_{min} = \frac{1}{2\pi} \cdot \frac{1}{\sqrt[6]{2} - 1} \approx 1.3. \quad (12)$$

4.3. Time-Constant Mismatch

Another important circuit imperfection is the time-constant mismatch. The absolute accuracy of the integrated capacitors and resistors can vary in a range of $\pm 10\%$ in the $0.5\mu m$ CMOS technology used. Thus, the time-constant can vary in a range of more than $\Delta\tau = \pm 20\%$. Considering this effect the inband noise at the output of the third order modulator results to:

$$IBN \approx \frac{\Delta^2}{12} \cdot \frac{\pi^6(1 + 6\Delta\tau)}{7a_1^2 OSR^7} \quad (13)$$

A time-constant variation of $\Delta\tau \leq 17\%$ results in a 3dB increase of inband noise power (Eq. 13).

4.4. Distortion

As far as distortion is concerned, primarily that of the first integrator has to be considered. The dominant sources of distortion are the input devices which are biased in moderate inversion. Furthermore, the bias current and the transconductance of the first integrator are determined by the dynamic range requirements of the overall A/D converter [4] shown in Fig. 8. This results in the following power consumption:

$$P \approx \frac{V_{dd}\hat{V}_{in}^2}{4R_{in}} \cdot \sqrt{\frac{1}{g_{m2}\, HD_3} \cdot (\frac{1}{R_{in}} + \frac{1}{R_{dac}})}. \quad (14)$$

Power minimization can be done by increasing R_{in} up to the thermal noise limit in the same way as R_{dac}. Moreover, the power consumption is reduced by a large g_{m2}. The transconductors in the second and third stage have more relaxed requirements on distortion.

4.5. Circuit Noise

In a third order $\Sigma\Delta$ modulator the noise power is dominated by circuit noise ($1/f$ noise and thermal noise). As Fig. 6 shows, circuit noise as well as other nonidealities in the first integrator occur unshaped at the output of the modulator. In contrast, errors of the second and third integrator,

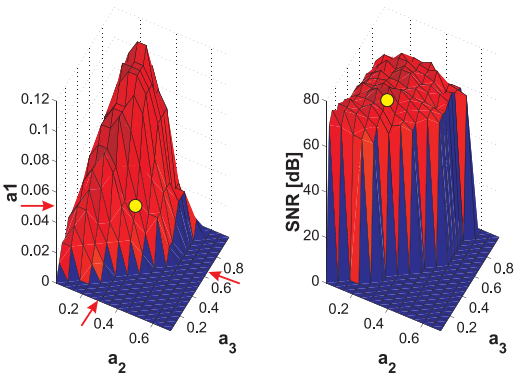

Figure 7. (a) Stability analysis of the 3rd-order $\Sigma\Delta$ modulator [7] for the NRZ feedback coefficients a_1, a_2 and a_3. (b) Resulting SNR for the stable coefficients a_1, a_2 and a_3.

will be shaped first and second order respectively. Thus the first integrator has to fulfil the noise requirements of the entire $\Sigma\Delta$ modulator.

5. Circuit Considerations

The effect of the low supply voltage on the total power consumption, noise contribution as well as on the input and output voltage swing will be specified in this paragraph. As a result the optimal operating point of the transistor implementation with respect to a minimal power consumption and noise can be found.

Lowering the supply voltage V_{DD} in an A/D converter demands a lower noise contribution $\bar{v_n}^2$ for the same dynamic range. This requires larger transconductances (Eq. (15)) and consequently higher bias currents.

$$\bar{v_n}^2 \propto \frac{1}{g_m} \propto \frac{1}{\sqrt{I_{DS}}} \tag{15}$$

Furthermore, $g_m = 2I_{DS}/V_{DS,sat}$. In low-voltage applications $V_{DS,sat}$ should be constant, thus $g_m \propto I_{DS}$. As a consequence, lowering the supply voltage V_{DD} in noise dominated and $V_{Ds,sat}$ critical circuits increases the overall power consumption. A key design parameter for the first integrator especially for low-voltage operation is the input and output swing (IS, OS), since $SNR \propto OS^2$. In order to combine the high gain and low-power requirements a single stage folded-cascode amplifier has been chosen. Furthermore, the input transistors as well as the output transistors are biased in moderate inversion with $V_{GS} - V_T$ in the range of 0 to $100mV$.

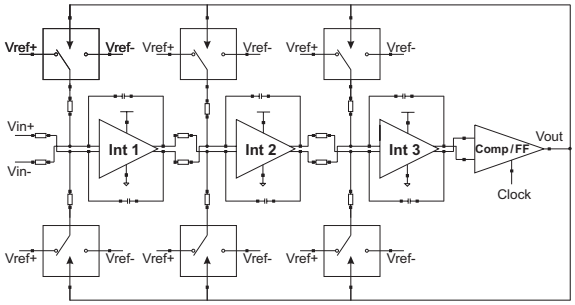

Figure 8. Implementation of the CT $\Sigma\Delta$ modulator.

6. Low-Power Third Order $\Sigma\Delta$ Modulator

To complete the design strategy the parameters that determine the performance (SNR) of the A/D converter have to be evaluated. Thus, these parameters can be set so that the desired resolution can be achieved.

In a 3rd-order $\Sigma\Delta$ modulator the SNR is limited by circuit noise. Consequently, the ADC resolution can be calculated with the following relationship. The input-referred noise power density is approximately :

$$S_i^2 \approx 8kT(R_{in} + R_{DAC} + \frac{2\ n_{e,th}}{3\ g_{m,in}}) + \frac{K_f\ n_{e,f}}{C_{OX}^2 WLf} \tag{16}$$

In (16) $n_{e,th}$ and $n_{e,f}$ describe the noise excess factors. Note that since the noise is not sampled until it has been filtered the aliased noise components are attenuated by noise shaping. Therefore, the input-referred noise power that appears in the baseband is equal to[2]:

$$\bar{v}_{in,therm}^2 = \frac{8kT\,a_{int}}{OSR\ R_{in}\ C_1}(R_{in} + R_{DAC} + \frac{2\ n_f}{3\ g_{m2}}). \tag{17}$$

The dynamic range of the $\Sigma\Delta$ modulator is determined by the ratio of the signal power $S = \hat{V}_{in}^2/2$ and the circuit noise power ($\bar{v}_{in,therm}^2$). Eq. (17) shows the different design parameters that can be used to obtain the required dynamic range. Reducing the supply voltage demands a lower thermal noise contribution for the same DR. This requires smaller resistances (R_{in} and R_{dac} respectively) and a larger transconductance and consequently higher bias currents. The complete circuit implementation is shown in Fig. 8.

The used CT integrator coefficients are given in Eq. (18) and the corresponding simulations are shown in Fig. 7:

$$\begin{aligned} a_{1_{NRZ}} &= 0.05 \quad & a_{1_{RZ}} &= 0.1 \\ a_{2_{NRZ}} &= 0.3 \quad & a_{2_{RZ}} &= 0.6 \\ a_{3_{NRZ}} &= 0.6416 \quad & a_{3_{RZ}} &= 1.2864. \end{aligned} \tag{18}$$

[2] In the following equation it is assumed that the amplifier has negligible flicker noise.

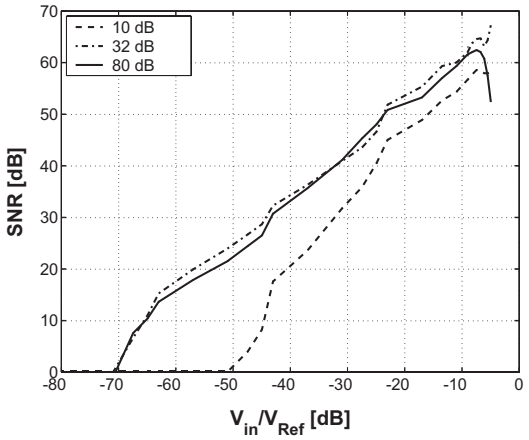

Figure 9. Simulated SNR as a function of the amplifier DC-gain A_V.

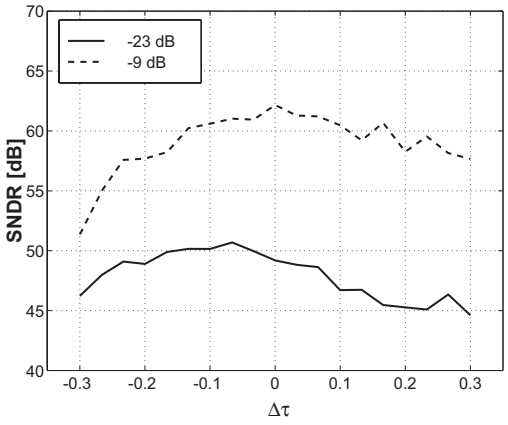

Figure 11. Impact of time-constant mismatch for different input signal powers on the $\Sigma\Delta$ modulator .

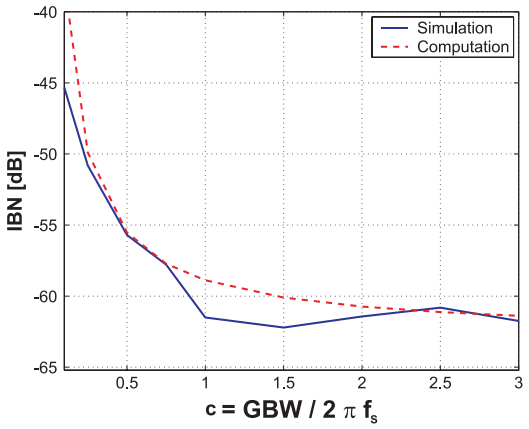

Figure 10. Influence of finite gain-bandwidth (non-dominant integrator poles) on the in-band noise (IBN) of the $\Sigma\Delta$ modulator.

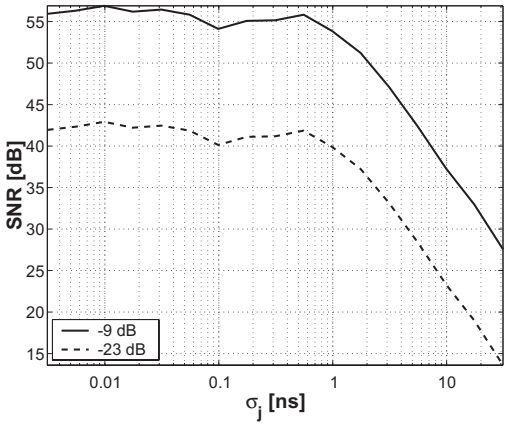

Figure 12. Influence of clock jitter σ_j on the entire CT $\Sigma\Delta$ modulator with RZ-DAC feedback scheme for different input signal powers.

Fig. 7a show sets of stable coefficients a_1, a_2 and a_3, whereas Fig. 7b exhibits the maximal achievable SNR respectively.

7. Simulation Results

7.1. Behavioral Simulation Results

In order to verify the previously derived theoretical results, behavioral simulations of the A/D converter considering the effects of finite gain, clock jitter, time constant mismatch and finite gain-bandwidth have been done using MATLAB.

The presented simulation results of the $1.5\ V$ 3rd-order CT $\Sigma\Delta$ modulator have been carried out for a sampling frequency of $1.6\ MHz$ and a fixed OSR of 32, yielding a signal bandwidth of $25\ kHz$. The applied input signal frequency is $5\ kHz$ for SNDR and $20\ kHz$ for SNR simulations and the inband noise is calculated from $500\ Hz$ on. The results are summarized in Fig. 9 to Fig. 12. Figure 9 shows the effect of leakage on the A/D converter resolution. In order to limit performance degradation the amplifier DC-

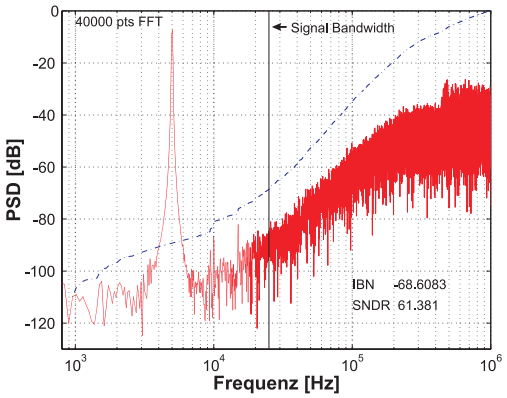

Figure 13. Power Spectral Density (PSD) and Inband-Noise (IBN) of CT $\Sigma\Delta$ modulator.

gain (A_V) has to be higher than $OSR = 32$.

The effect of non-dominant integrator poles on the modulator inband noise power is determined by simulations as shown in Fig. 10. Figure 10 displays that the behavioral simulation results fit very good with the computation (Eq. 10). Furthermore, Figure 10 shows that GBW should be equal to the sampling frequency ($c \approx 1$) to preserve the desired resolution.

The effect of time-constant mismatch on the entire A/D converter is shown in Fig. 11. As can be seen integrator time-constant variations of $\Delta T_S = \pm 20\%$ result in a maximal SNDR degradation of $5dB$. This result is comparable to the value of Eq. 13.

Moreover, Fig. 12 demonstrates the impact of clock jitter on the overall modulator performance. The major source of jitter error is the feedback current. Since the feedback current is subtracted from the input signal, the jitter error power adds directly to the input signal. The designed third order modulator requires clock jitter below 0.5 nanoseconds.

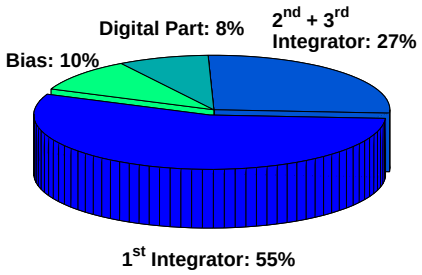

Figure 14. Partitioning of the overall power consumption for the third order modulator.

Signal Bandwidth	$25\ kHz$
Sampling Frequency	$2.4\ MHz$
Dynamic Range	$75\ dB$
peak $SNDR$	$65\ dB$
Power Consumption	$230\ \mu W$
FOM	$90 \cdot 10^{-6}$
Technology	$0.5\ \mu m$ CMOS

Table 2. Expected performance summary of the 3rd-order $\Sigma\Delta$ A/D converter.

7.2. Transistor-Level Simulation Results

A more realistic verification can be done by using transistor-level simulations. The CADENCE design environment with the simulator SPECTRE was applied. Thus, finite input and output resistances, finite slew rate and settling time, additional delay times, parasitic capacitors and noise sources can be taken into consideration. The results of the transistor-level simulations of the implemented modulator are shown in Fig. 13 and Fig. 14.

All three integrators as well as the DAC and also the comparator are modelled on transistor-level. Figure 13 shows the power spectral density and inband-noise for an input signal of $-8dB$ @ $5kHz$. The second and third harmonic distortion are well below $-90dB$ and $-80dB$ respectively. The resulting inband-noise is $-69dB$ and the SNDR is $62dB$. Another advantage of transistor-level simulations is detailed information about the power consumption of any A/D converter system block. Figure 14 shows the partitioning of the entire power consumption on the different building blocks. The entire A/D converter provides a peak SNDR of $65\ dB$ and a dynamic range of approximately $75\ dB$. The maximum stable input signal is about $-6\ dB$, half of full-scale. The simulated performance of the entire A/D converter is summarized in Tab. 2.

The power efficiency of various A/D converters with different resolutions and sampling rates can be compared using again the FOM. Figure 15 plots the power consumption over the signal bandwidth versus the dynamic range for some recently published CMOS A/D converters. The power dissipation used in the computation does not include the decimation filter, nor the antialiasing filter. Furthermore, Fig. 15 demonstrates that the design strategy results in a good power efficiency.

8. Modulator Layout

The A/D converter was implemented in a $0.5\mu m$ triple-metal standard analog CMOS technology ($V_{Tn} = 0.58mV, V_{Tp} = 0.62mV$). The required area is less than

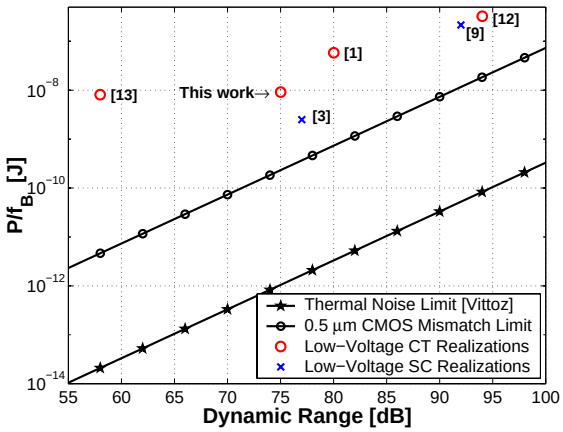

Figure 15. Power consumption over the signal bandwidth vs. dynamic range of recent low-voltage $\Sigma\Delta$ A/D converters.

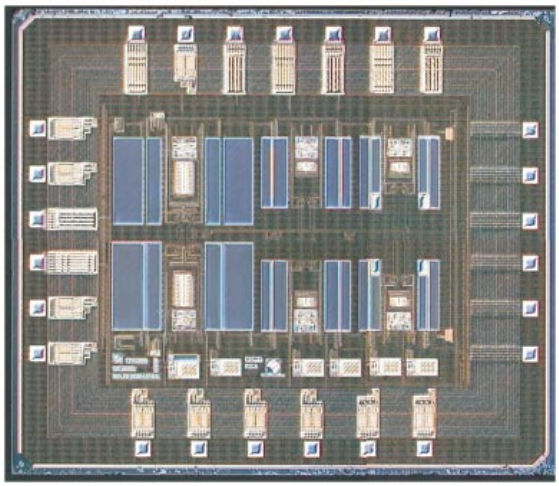

Figure 16. Chip photo

$1.2mm^2$ with the first integrator consuming more than 50% of the total area (Fig. 16). The modulator was implemented twice. The lower one was especially designed for testability.

9. Conclusion

A rapid prototyping design strategy for a low-voltage/low-power third order continuous-time $\Sigma\Delta$ modulator has been presented. The implementation has been done without using a multi-threshold technology or voltage multiplication. An improved method was used to find the optimal $\Sigma\Delta$ modulator implementation with respect to a minimal power consumption. The influence on circuit nonidealities like integrator leakage, distortion and noise on the overall A/D converter has been studied and verified by simulations. Furthermore, the effect of low-supply voltage on the integrator as well as on the entire $\Sigma\Delta$ converter has been shown. The modulator has been designed in a $0.5\mu m$ CMOS technology. As a result the low-power consumption shows that the proposed design strategy is a good approach for low-voltage $\Sigma\Delta$ A/D converter realizations.

References

[1] B. B. B.A.Wooley. The Design of Sigma-Delta Modulation Analog-to-Digital Converters. *IEEE Journal of Solid-State Circuits*, 23(6), December 1988.

[2] F. M. et al. *Top-Down Design of High-Performance Sigma-Delta Modulators*. Kluwer Academic Publishers, 1999.

[3] J. C. et al. Excess Loop Delay in Continuous-Time Delta-Sigma Modulators. *IEEE Transactions on Circuits and Systems -II*, 46(4), April 1999.

[4] L. B. et al. Design for Optimum Performance-to-Power Ratio of a Continuous-time $\Sigma\Delta$ Modulator. *ESSCIRC, Proceedings of the 25^{th} European Solid-State Circuits Conference*, September 1999.

[5] V. P. et al. A 900-mV Low-Power $\Sigma\Delta$ A/D Converter with 77-dB Dynamic Range. *IEEE Journal of Solid-State Circuits*, 33(12), December 1998.

[6] E. Jury. *Theory and Applications of the Z-Transform Method*. John Wiley & Sons, 1964.

[7] L. Risbo. $\Sigma-\Delta$ Modulators-Stability Analysis and Optimization. *PH.D Thesis, Technical University of Denmark*, 1994.

[8] O. Shoaei. Continuous-Time Delta-Sigma A/D Converters for High Speed Applications. *IEEE Journal of Solid-State Circuits*, 31(12), December 1996.

[9] E. van der Zwan; et al. A 0.2-mW CMOS $\Sigma\Delta$ Modulator for Speech Coding with 80 dB Dynamic Range. *IEEE Journal of Solid-State Circuits*, 31(12), December 1996.