Crosstalk Noise in Future Digital CMOS Circuits

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Abstract

This paper presents simulation results for crosstalk noise in future CMOS generations down to 35 nm features. The noise oltage is calculated from circuit simulations with lumped RLC networks and static CMOS cells. A static noise margin is derived from inverter characteristics of NAND and NOR gates and a critical wire length is calculated from considering statistical variations in the chip manufacturing process. The model agrees well with measurements on a quarter micron testchip and predicts a drastic drop of critical wirelengths to 50-60 µm after the 100 nm technology generation .

1. Introduction

In CMOS technologies of 0.35 µm and above noise immunity has not been much of a problem for purely digital applications. While noise margins have always been of special concern for analog and mixed signal designs, the large distance between the logical 1 and logical 0 voltages in digital circuits of feature sizes above quarter micron has mostly prevented occasional noise glitches to propagate beyond the next logical evaluation node of the circuit.

However, for very deep submicron generations with decreasing wire spacing and enhanced signal slew rate, capacitive and also inductive cross coupling between adjacent wirelines will lead to enhanced noise levels, which could disturb the proper function of the digital circuit, especially since the supply voltage of those future technology generations will be significantly lower than today.

This contribution is organized as follows: Section 2 will describe a simulation model, which allows reliable noise calculation for future CMOS generations from the technology predictions given in the ITRS roadmap [1]. This model is calibrated by extensive measurements using a quarter micron test chip, and is then applied to predict crosstalk noise data for future technology generations down to 35 nm feature size. In section 3 we calculate the noise margins for those future technologies and extract critical wire lengths for cross talk immune designs. Finally in section 4 we end with a summary of our results.

2. Crosstalk Noise

2.1. Simulation Model

Our simulations were performed with our inhouse circuit simulator TITAN [2] using a lumped element representation of 20 RLC elements driven by a CMOS inverter. However, for the local and intermediate metal levels investigated in this study, we found that the wire inductances were very small and did not influence the results to a noticeable extent. Inductive effects only play a role for the global or fat wires running across the whole chip, which carry a high current. The wire dimensions for future technology generations were taken from the ITRS roadmap and the specific capacitances were calculated using analytical approximations given by Delorme [3]. For some cases we checked the accuracy of these formulae by comparison to 2 D numerical results from [4] and found an agreement within 15%. The MOSFET currents were taken from published results on future technology generations [5,6] and described by an appropriate parameter set.

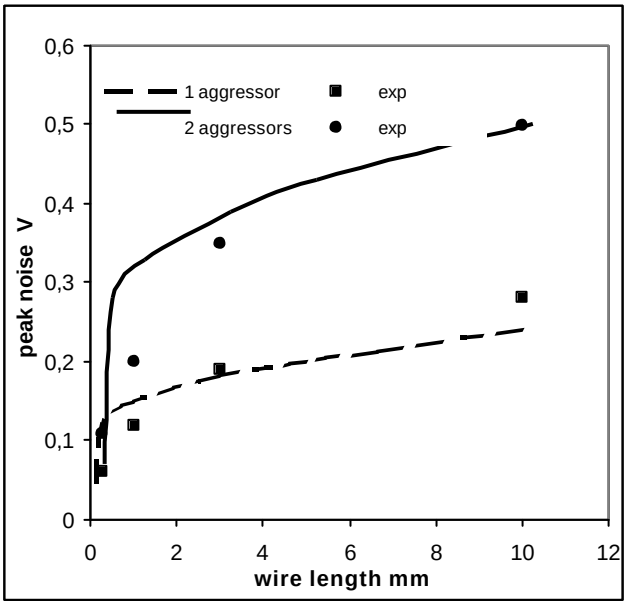

Figure 1. Crosstalk noise as a function of wire length. Experimental results on a 0.25µm testchip and simulation

2.2. Calibration for 0.25 µm technology

An extensive body of measurements using a quarter micron testchip was used to verify the accuracy of our approach. Details about the measurement method and the test strutures investigated are given in [7]. Fig. 1 –3 show the agreement of our model with the experimental data for noise glitches, crosstalk duration and crosstalk induced delay as a function of wire length.

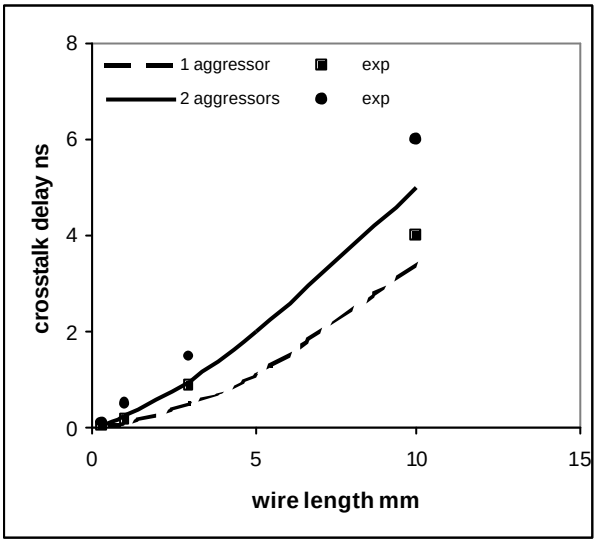

Figure 2. Crosstalk induced delay as a function of wire length. Experimental results on a 0.25µm testchip and simulation

2.3 Prediction for future CMOS generations

We investigated two different arrangements of victim and agressor lines for possible crosstalk noise, as depicted in Fig. 4. While the arrangement of Fig.4 a, where the signals in victim and agressor run in parallel over the total length, might be the predominant structure in global wires connecting different circuit blocks on a chip, the arrangement of Fig.4b (many short agressor lines acting onto the same long victim) might be the worst case for intermediate and local chip wiring.

The wire dimensions for future technology generations were taken from the ITRS roadmap [1]. For this study we assumed copper interconnects from an intermediate metalization level and a low k dielectric, detailed data are given in Table1.

Technology	Width	Space	thickness	ε
100nm	170 nm	170 nm	410 nm	1.9
70 nm	120 nm	120 nm	300 nm	1.7
50 nm	80 nm	80 nm	220 nm	1.5
35 nm	60 nm	60 nm	170 nm	1.5

Table 1 Interconnect dimensions for technology generations considered in this paper after [1]

Fig.5 shows the results for the maximum noise peak as a function of wire length in future technology generations down to 50 nm. We see that the multiple agressor arrangement leads to peak noise voltages above 20% of Vdd for all wires longer than 0.2mm. For the single aggressor arrangement peak noise stays below 20% Vdd for wires shorter than 4 mm for the 100nm technology, but for further generations it rises to 30-40% for wires above 1 mm.

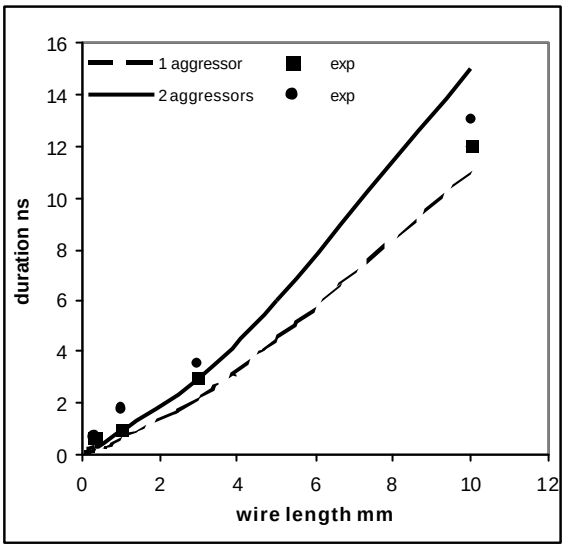

Fig. 3 Duration of crosstalk peak for a 0.25µm technology Experimental results on a 0.25µm testchip and simulation

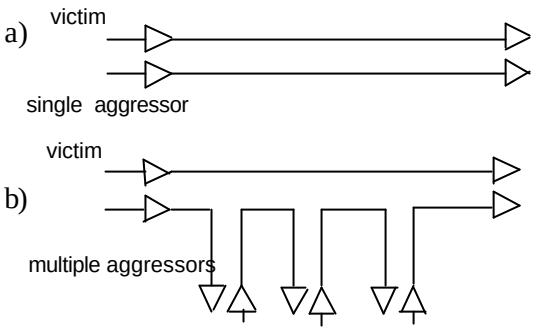

Fig. 4 Two different aggressor arrangements considered in this paper

3. Noise Margin and Critical Wirelength

3.1 Static noise margin

To get a measure for the maximum allowable noise voltage we use the stability criterion of Shepard [8]. Consider the transfer characteristic of a static logical gate as shown in Fig.6. We define the switching points at which the tranfer characteristic exceeds unity gain as the low and high stability points V_{iL} and V_{iH}, i.e. where we have

$$\left|\frac{\partial Vout}{\partial Vin}\right| = 1.0$$

As a static noise margin we get the difference between the worst case output and the worst case input taken from all gate cells used in this design

V_{nmL} = min{V_{iL}|all cells}– max {*Vout* (V_{iH})|all cells}
V_{nmH} = min{*Vout* (V_{iL}) |all cells}– max{ V_{iH} |all cells}

From this definition a proper function of the circuit can be guaranteed as long a the maximum crosstalk noise coupled into wirelines between the cells stays below the threshold V_{nmL} for a victim held at low voltage, and below V_{nmH} for a victim at high voltage.

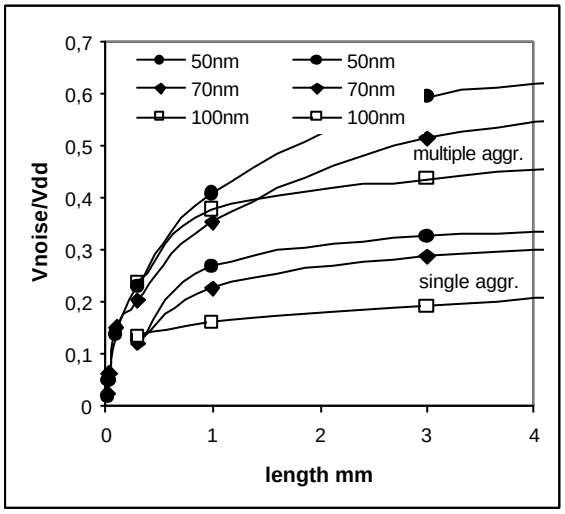

Figure 5. Crosstalk noise peak relative to Vdd for different CMOS generations and for two aggressor arrangements

Table 2 gives the calculated static noise margins for all of the future technologies considered in our study. As typical cells we have taken three-input NAND and NOR gates in all three technologies The difference between the high and low levels depends on the detailed optimization of the NMOS and PMOS widths in the cell library. We will use the average value V_{av} in this study to become independent of those details.

Technology	Vdd	Vnml	Vnmh	Vav
100nm	1.35 V	0.45 V	0.47 V	0.46 V
70 nm	0.75 V	0.30 V	0.16 V	0.23 V
50 nm	0.55 V	0.25 V	0.11 V	0.18 V
35 nm	0.45 V	0.22 V	0.10 V	0.16 V

Table 2: Supply voltage and static noise margins for future CMOS generations

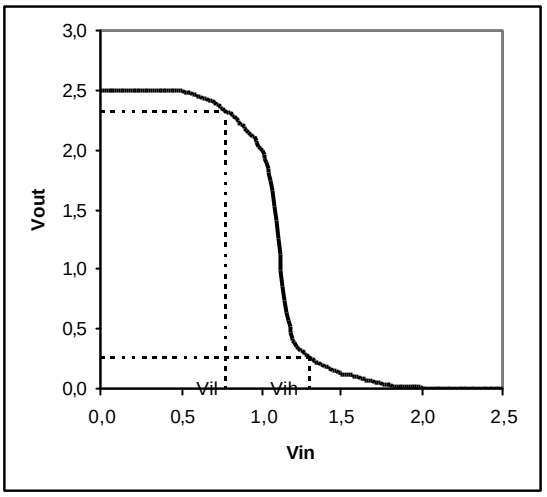

Figure 6. Definition of noise margins for a three input NAND gate from quarter micron technology

3.2 Statistical fluctuation of parameters

It is well known that for a high yield and a very large number of elements in a circuit, statistical fluctuations of critical dimensions and parameters must be taken into consideration. Thus, even if the nominal noise margins are above the noise voltage coupled into a wire with a nominal distance from the neighbouring wire, we still remain with some statistical probability of crosstalk failure in a small fraction of devices. Though it will be possible to identify the chips with faulty devices by a proper crosstalk aware test pattern, the effect will drastically reduce the yield of future technologies, if it is not avoided by limiting the maximum lengths of parallel running wirelines.

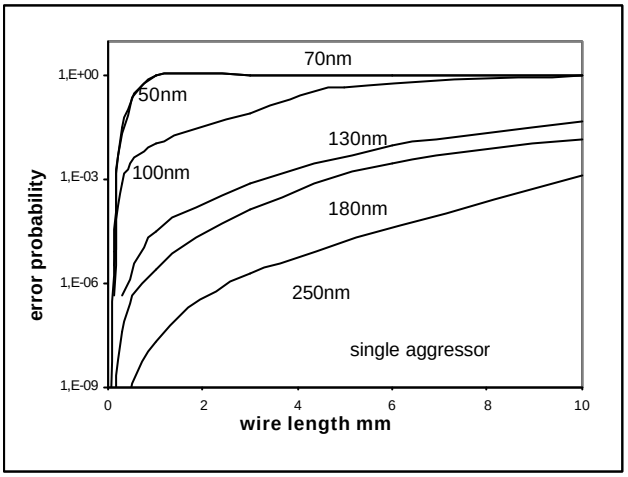

Figure 7: Probability of crosstalk faults as a function of wirelength for different CMOS generations. Single agressor arrangement

In Fig. 7 and 8 we predict the error probability for crosstalk failures as a function of wirelength for some future technology generations. Here we assumed a 10% variation in crosstalk noise due to metal etching uncertainties, and a threshold uncertainty of 60mV, 40 mV, 30mV and 25mV (1 σ) for the three technologies 100nm, 70nm, 50nm, and 35 nm, respectively.

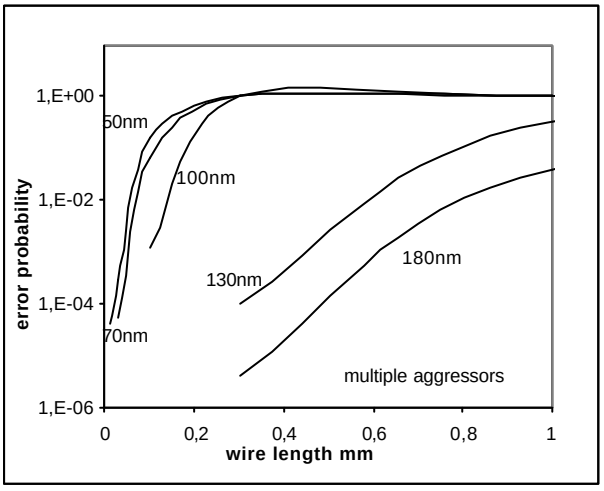

Figure 8. Probability of crosstalk faults as a function of wirelength for different CMOS generations. Multiple aggressor arrangement.

3.3 Crititcal wire lengths

The results from our model have been used to derive curves for the critical wire lengths L_{crit}, which must not be exceeded in a design to assure a crosstalk immune function. We define L_{crit} as the victim length at which the probability of crosstalk error is 10^{-2} . In Fig. 9 we plot the critical lengths as a function of technology generation. Two cases have been considered. The upper curve refers to a pair of wires which run in parallel over the entire length as in a bus structure (single aggressor). The lower curve, which gives much smaller values of L_{crit}, however, is for the case, where we have 4 identical agressors, each of one quarter of the total length, which attack the victim along its total length one after the other (multiple aggressor, Fig. 4b). We think that the lower curve might be more realistic for the worst case in real layouts. Nevertheless, both cases seem to indicate, that there is not much further reduction in L_{crit} after the 70 nm technology generation.

4. Conclusions

In this contribution a prediction of the magnitude of crosstalk noise in future CMOS technologies has been presented. The multilevel metalization schemes to be used in those technologies allow the differentiation between basically three classes of interconnects: local, intermediate and global. It is expected that the intermediate interconnects (metallayer 3 – 4) studied in this contribution will pose the most severe crosstalk problems in future CMOS generations. Our investigations found out that those interconnects will be limited by crosstalk lengths of 60µm and below especially for the smallest feature size from the 35 nm technology generation studied here. We expect that for these interconnects sophisticated design schemes (e.g. as described in [9]) will be required to make sure that only uncritical signals are routed in close neighborhood or otherwise a large spacing or a shielding scheme must be used.

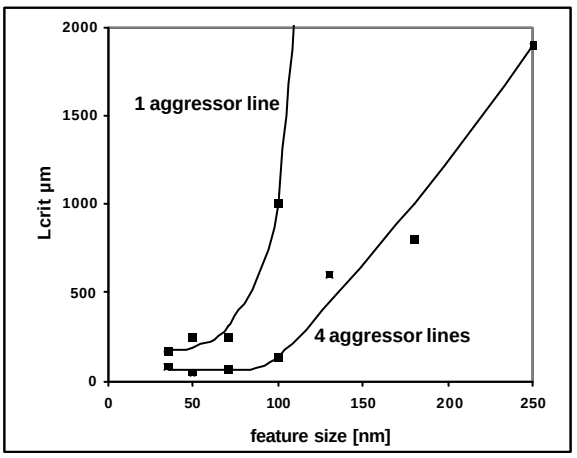

Figure 9. Critical wire length for CMOS technology generations of different feature size

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