Incorporation of Hard-Fault-Coverage in Model-Based Testing of Mixed-Signal ICs

Carsten Wegener and Michael Peter Kennedy
University College Cork, Lee Maltings, Prospect Row, Cork, Ireland
carsten_wegener@email.com Peter.Kennedy@ucc.ie

Abstract—The application of the Linear Error Mechanism Modeling Algorithm (LEMMA [1]) to various DAC and ADC architectures has raised the issue of including hard-fault-coverage as an integral part of the algorithm.

In this work, we combine defect-oriented functionality tests and specification-oriented linearity tests of a Mixed-Signal IC to save test time. The key development is a novel test point selection strategy which not only optimizes the INL-prediction variance of the model, but also satisfies hard-fault-coverage constraints.

Introduction Using well-established system identification methods to cut the costs of testing mixed-signal ICs has recently attracted much research effort [2, 3]. The ultimate aim is to automate the development of test procedures and to ensure an optimal trade-off between test time per part and the confidence of the test result. A paradigm, called the Linear Error Mechanism Modeling Algorithm has been developed and a tutorial introduction of this algorithmic approach is given in [1].

Strategies to develop linear models for parametric-faults, such as the integral nonlinearity (INL) of a DAC or ADC, caused by spreads in on-chip component values have been independently implemented in two software packages [4, 5]. Both implementations select test points by unconstrained minimization of the prediction variance of the linear model. The 12-bit DAC we consider is targeted at low-cost control-loop applications where the time spent on testing this part is critical.

Traditionally, functionality tests are performed before verifying that the specifications of the analog part of the circuit are met. In [6] it has been pointed out that both aspects of "faulty devices: excessive process deviations and spot defects... must be accounted for when developing and evaluating general test methodologies." We go even further, by suggesting to interweave functionality and linearity tests in order to save test time, which adds value to our model-based test methodology, called LEMMA. During the poster presentation this will be demonstrated in detail for our 12-bit example DAC, where hard-fault-coverage is embedded in the linearity test by means of a novel test point selection strategy.

The set of hard-faults we consider here has the property that any fault becomes apparent in the full-factorial measurement, i.e. for every fault, there exists at least one code c^* such that $\mathrm{INL}(c^*)$ does not meet the specifications. The Fault-Coverage problem, that some hard-faults are not necessarily detected, arises for all test methodologies based on reduced sets of test points, of which LEMMA is an example.

Results An all-codes test would detect all faults that cause a violation of the circuit specifications, but the test time is prohibitive for production purposes. The application of the standard LEMMA method cuts the number of test points required for the specification test down to 64, but an additional set of 62 test points is required to ensure basic functionality of the device under test.

By including the constraints of hard-fault coverage into the test point selection strategy; with 66 test points we can guarantee basic functionality of the device under test and while reaching a level of accuracy for the result of the specification test that is comparable with that of the standard LEMMA test.

Test Method	# Test Pts	e_{INL}
All-codes	3999	0.32
LEMMA	64	0.50
LEMMA+FC	66	0.46

Table 1: For various test methods: Test effort and uncertainty (e_{INL} in LSBs) of the test result.

References

[1] A. Wrixon and M.P. Kennedy, "A rigorous exposition of the LEMMA method for analog and mixed-signal testing." IEEE Trans. IM, October 1999.

[2] G.N. Stenbakken and T.M. Souders, "Developing linear error models for analog devices." IEEE Trans. IM-43(2), pp. 157-163, 1994.

[3] P.D. Capofreddi and B.A. Wooley, "The use of linear models in A/D converter testing." IEEE Trans. CAS-I, vol. 44(12), pp. 1105-1113, Dec. 1997.

[4] M.P. Kennedy et al., "The LEMMA developer's toolbox: semi-automated test development for analog and mixed-signal circuits." In Proc. ISCAS'98, vol. II, pp. 410-413, Montery, CA, 31 May-3 June 1998.

[5] G.N. Stenbakken, T.M. Souders and A.D. Koffman, "Software to optimize the testing of Mixed-Signal devices." In Proc. 5^{th} IEEE Int. Mixed Signal Testing Workshop, British Columbia, Canada, June 1999.

[6] S.J. Spinks and I.M. Bell, "Beyond Fault Coverage: Estimating test quality for comparing test methodologies or evaluating testability." In Proc. 3^{rd} IEEE Int. Mixed Signal Testing Workshop, Seattle, WA, USA, June 1997.