Improving the Error Detection Ability of Concurrent Checkers by Observation Point Insertion in the Circuit Under Check

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Abstract

A heuristic design-for-checkability method based on observation point insertion in the Circuit Under Check (CUC) is proposed to increase the error detection ability of Concurrent Checkers (CC). In particular, at least 99% of error detection is obtained for parity checkers and almost all ISCAS'85 benchmark circuits by inserting 2-5 groups of observation points compacted by parity trees.

1. Introduction

The linear compaction method proposed in [1] for parity checkers is based on partitioning of the set of primary outputs of the CUC into disjoint groups. The outputs of ISCAS'85 benchmark circuits were partitioned into 3-5 groups to achieve 98% of error detection.

In this paper, the following general problem is considered: Given a combinational CUC and a conventional CC, transform the CUC and/or the CC in order to improve the error detection ability of the checker as much as possible at a low hardware overhead**.** The probabilistic measure P_{ed} defined in [2] as error detection probability is used as a quantitative measure of error detection ability of a CC. Since in many important applications over 99% of error detection ability is mandatory, the problem of designing CC with very high error detection ability is of considerable interest.

2. Main approach

Groups of observation points are selected in the CUC successively by traversing from the primary outputs. Each group of observation points is compacted by a parity tree and the outputs of all parity trees are compared with the predicted values of their complements by means of a Two-Rail Checker. The process of selecting groups of observation points is continued while the error detection probability for the checker does not exceed 0.99, thus enabling to achieve at least 99% of error detection. The complexity of our approach is quadratic with respect to the number of lines of the CUC and linear with respect to the number of primary outputs. The proposed method may be successfully combined with the method [1].

3. Experimental results

The experimental results for parity checkers and almost all ISCAS'85 benchmark circuits with 10.000 pseudorandom input patterns are listed in the table.

References

[1] M. Seuring, M. Gössel, and E. Sogomonyan, **"**A Structural Approach for Space Compaction for Concurrent Checking and BIST. Proc. 16th IEEE VLSI Test Symposium, 1998.

[2] V.A.Vardanian, "Exact Probabilistic Analysis of Error Detection for Parity Checkers". Proc. 15th IEEE VLSI Test Symposium, 1997.

Circuit	Inputs	Outputs	Groups	Observation Points	Ped (%) Initial	Ped (%) Final	Increase (%)
C432	36	7	4	12	67.99	99.85	31.86
C499	41	32	2	17	90.37	100.0	9.63
C880	60	26	3	39	91.84	99.55	7.71
C1355	41	32	2	17	94.53	100.0	5.47
C1908	33	25	3	25	85.11	99.05	13.94
C2670	233	140	3	39	68.47	99.84	31.37
C3540	50	22	5	91	81.44	99.38	17.94
C5315	178	123	2	135	72.22	99.04	26.82
C7552	207	108	4	143	90.40	99.13	8.93