Exploiting Hierarchy for Multiple Error Correction in Combinational Circuits*

Dirk W. Hoffmann

Institute for Computer Engineering
University of Tübingen
D-72076 Tübingen, Germany
hoff@informatik.uni-tuebingen.de

Thomas Kropf

Institute for Computer Engineering
University of Tübingen
D-72076 Tübingen, Germany
kropf@informatik.uni-tuebingen.de

Boolean equivalence checking has turned out to be a powerful method for verifying combinational circuits and is already an integrated part of the design cycle. If equivalence checking fails, *Design Error Diagnosis and Correction* (DEDC) is performed. DEDC tries to locate and correct design errors fully automatically and can therefore considerably speed up the whole design cycle.

The methods can roughly be divided into three classes: *ATPG based* approaches (e.g. [4]), *structure based* approaches [3], and *logic based (symbolic)* approaches (e.g. [1]). Most approaches rely on the "single error assumption" and cannot be applied if multiple errors occur in a circuit. This is a hard restriction for practical applications as the average number of design errors is usually greater one. However, multiple error rectification is a challenging task since the search space grows exponentially with the number of design errors.

Our method is a *symbolic method* for *multiple* error rectification of combinational circuits and further development of [1] that can correct single errors, only.

The main characteristics of our approach can be summarized as follows:

- Our approach works on hierarchical netlist. Hierarchy is a crucial issue of our method and is exploited to prune the search space considerably. This is a novel approach since all other methods proposed in the past work on flat netlists only.
- Our method is based on symbolic techniques. Thus, no error model has to be assumed and arbitrary design errors can be detected.
- Computed solutions are weighted by a cost function in order to find a minimal solution – a solution that requires minimal number of modifications in the implementation.
- Our rectification procedure is compatible with the tri-state elimination method in [2] and circuit abstractions (see [1]).
- Our rectification procedure is now integrated part of the AC/3 equivalence checker and circuit rectifier.

The following table shows some experimental results comparing our approach with the standard rectification algorithm.

size	no. of gates	ref. steps	rect. time (s)	standard appr. (s)	speed up factor
Cascade of carry look ahead adders, 2 errors:					
4	18	6	0.08	0.68	8.5
8	44	11	0.38	8.17	21.5
16	88	21	4.17	181.39	43.5
32	240	21	5.36	640.52	119.5
64	480	19	15.43	> 1 h	239.5
128	960	68	332.18	> 4 h	479.5

References

[1] D. W. Hoffmann and T. Kropf. Automatic error correction of large circuits using boolean decomposition and abstraction. In *Proceedings of the Conference on Correct Hardware Design and Verification Methods (CHARME)*, Bad Herrenalb, Germany, September 1999. IFIP WG 10.5.

[2] D. W. Hoffmann and T. Kropf. Automatic error correction of tri-state circuits. In *Proceedings of the 17th IEEE Internation Conference on Computer Design (ICCD)*, Austin, TX, October 1999. IEEE.

[3] S.Y. Huang, K.C. Chen, and K.T. Cheng. Error correction based on verification techniques. In *Proceedings of the 33rd Design Automation Conference (DAC)*, 1996.

[4] A. Veneris and I. N. Hajj. Correcting multiple design errors in digital VLSI circuits. In *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, Orlando, Florida, USA, May 1999.

*This work is supported by the ESPRIT LTR Project 26241 (PROSPER)