Effective Low Power BIST for Datapaths

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Abstract

Power in processing cores (microprocessors, DSPs) is primarily consumed in the datapath part. Among the datapath functional modules, multipliers consume the largest amount of power due to their size and complexity. We propose a low power BIST scheme for datapaths built around multiplier-accumulator pairs. The target is low average power dissipation between successive test vectors. This is achieved by taking advantage of the regularity of multiplier modules and achieving very high fault coverage by a linear-sized test set with as small as possible input switching activity. The proposed BIST scheme is more efficient than pseudorandom BIST for the same high fault coverage target. Up to 77.25% power saving is achieved in the set of experimental results provided in the paper.

1 Introduction

Power consumption is a serious consideration in IC design and testing. Low power consumption prolongs the life of the batteries in portable systems, increases the length of the operating periods, and requires less expensive packages and cooling mechanisms, thus decreasing the system cost [1].

Circuit activity that leads to power consumption in CMOS circuits is significantly higher during test or self-test intervals [2]. Particularly, in Built-In Self-Test (BIST) a large number of uncorrelated pseudorandom test vectors are applied to the circuit causing a significantly higher circuit activity compared to circuit activity during normal mode of operation.

2 The Proposed BIST Architecture

We focus on low power BIST for the central operating part of embedded processors and DSPs, the datapath. In such circuits, power is consumed in the datapath modules and particilarly in the multipliers. We propose a deterministic BIST TPG approach for multiplier-accumulator pairs which is much more efficient compared to pseudorandom BIST in terms of power consumption.

The BIST architecture is based on a linear-sized test set that achieves a very high fault coverage for any multiplier size applying very low circuit input activity. Only one of the operand bits changes in successive test vectors and thus the multiplier array is tested in slices. This way a potentially smaller test set is "expanded", in order to achieve very small circuit activity with the same high fault coverage. The benefit of this architecture is a very large reduction in the average power consumption per vector pair compared to classical pseudorandom BIST. BIST output data compaction is performed using the existing accumulator of the datapath.

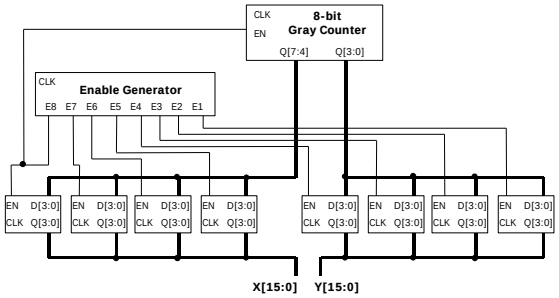

Figure 1: Low power TPG

The TPG of the proposed BIST scheme is shown in Figure 1. According to this scheme only one bit changes in the entire operands of the multiplier. The overall test set size in this scheme is **256 N/2**, where **N** is the datapath width. An 8-bit counter is employed in this scheme operating as a Gray counter which is always the straightforward solution for power reduction. The 8-bit Gray counter generates a new value when the previous value has been loaded in the entire multiplier operands. During each clock cycle a 4-bit part of the multiplier operands is loaded with a counter output (the 4 low order bits are loaded to the Y operand while the 4 high order bits are loaded to the X operand). The **Enable Generator** block generates a set of enable signals, that determine the loading of the 4-bit patterns in the registers (only one 4-bit part is loaded at a time). This configuration is used in the carry-save, carry-propagate multipliers while for Booth encoded tree (Wallace) multipliers, X receives 3-bit repetitive patterns and the Y operand receives 5-bit ones.

3 Experimental Results and Comparisons

In the comprehensive set of simulations performed we investigate different implementations of the modules (standard carry-save array multiplier - CSA, Booth encoded Wallace tree multiplier - BWM, carry lookahead adder - CLA, Brent-Kung adder - BKA) and we compare the proposed architecture with pseudorandom BIST with a primitive polynomial LFSR TPG running for 500 clock cycles in all cases. We calculate power dissipation using a commercial power calculation tool, the **DesignPower**™ provided by **Synopsys** [3] with exact delay models for the cells and wires. We have implemented 16-bit architectures for the multiplier-adder scheme. All designs were implemented using a 0.8 micron double-metal 5V CMOS standard cell library provided by **AMS**. The circuit frequency was 10 MHz. Results are shown in the following Table. TPG denotes the TPG used, columns MULT and ADD denote the multiplier and adder architectures, FC denotes the fault coverage, HW denotes the hardware overhead, and PO denotes the average power consumed for a pair of test vectors in each method. All calculations include the TPGs, the compactors and the circuits under test.

TPG	MULT	ADD	FC	HW	PO
LFSR500	CSA	CLA	100.0	6.75	19.86
PROPOSED	CSA	CLA	100.0	10.47	5.06
LFSR500	CSA	BKA	100.0	6.91	19.31
PROPOSED	CSA	BKA	100.0	10.70	4.85
LFSR500	BWM	CLA	100.0	7.58	18.71
PROPOSED	BWM	CLA	99.9	11.75	4.35
LFSR500	BWM	BKA	100.0	7.78	18.15
PROPOSED	BWM	BKA	99.9	12.05	4.13

Table 1: Experimental Results

References

[1] M.Pedram, "Power Minimization in IC Design: Principles and Applications", ACM Trans. on Design Automation of Electronic Systems, vol. 1, no.1, pp. 3-56, 1996.

[2] Y.Zorian, *"A Distributed BIST control scheme for Complex VLSI devices"*, in Proc. of the 11th IEEE VTS, pp. 4-9, 1993.

[3] Synopsys Inc., *"Power Products Reference Manual"*, ver. 1998.08, August 1998".