A Versatile Built-In Self Test Scheme for Delay Fault Testing

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Abstract

A new Built–In Self Test (BIST) scheme is presented that can be used for both off-line production or periodic testing of delay faults as well as for concurrent detection of faults causing signal delays in the field. The scheme is based on the I_{DDT} monitoring of the outputs of the circuit under test (CUT). The proposed scheme has minimal impact on the performance and silicon area of the design since the same response verifier circuit is used for both off-line and concurrent detection of errors in the field.

The BIST architecture and technique

Timing-related failures prevent the circuit from functioning at-speed causing propagation delay to be less than or more than specified limits. Such delay variations are modeled by delay faults. Delay faults are critical in deep sub-micron technologies. Detection of delay faults requires at-speed testing. BIST schemes targeting delay faults useful for both off-line as well as on-line testing have not presented in the open literature.

In this paper we present a new BIST scheme for delay fault testing. We will show that the test response verifier circuit of the proposed BIST circuit can also be used for concurrent detection of faults causing signal delays in the field. Furthermore, the proposed technique has the advantage to cover delay faults causing larger than expected as well as shorter than expected delays in a CUT.

In the proposed BIST scheme any already known test pattern generator (TPG) for delay faults can be used. As response verifier a transition detection unit (TDU) is used, Fig. 1. A TDU based on $I_{SS}(I_{DD})$ transition current monitoring, using a current sensor, is adopted for the detection of delay faults. The TDU has a single output E which indicates the detection or not of a transition at the outputs of the CUT.

According to this approach, every line under observation feeds a single dummy buffer. A built-in current sensor (BICS) at the power supply of these buffers is used to sense an I_{SST} current, Fig. 1. The signal ENB is used to set the BICS to the sense mode of operation (ENB=high). The sensor detects any signal transition on the lines that feed the dummy buffers. Considering the timing waveforms of Fig. 2, in the test mode of operation the TPG applies successively test vectors to the CUT in predefined time intervals (G-CLK) according to the CUT specifications. A delay fault of the CUT that causes a transition in the period T_1-T_2 or T_3-T_4 will result in the activation of the TDU and an error indication signal on E.

Furthermore, the proposed BIST architecture can also be used for detecting faults causing signal delays in the field. In that case the TPG is inactive and the CUT is fed by the normal operation mode vectors by the primary inputs. We note that during period $T_3 - T_4$ the BICS detects a delayed signal transition due to input I_j or a fast input transition due to input I_{j+1}. A problem that may arise concerns the longer than expected delay faults where their delay time exceeds the time interval during which the TDU is active. These faults are undetectable.

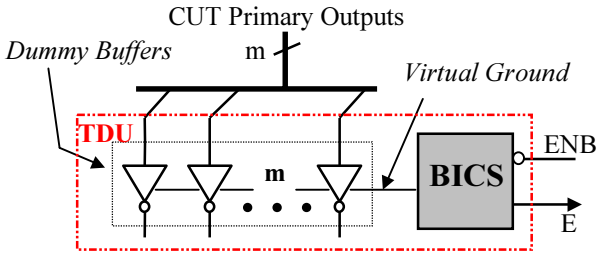

Figure 1. The TDU block diagram

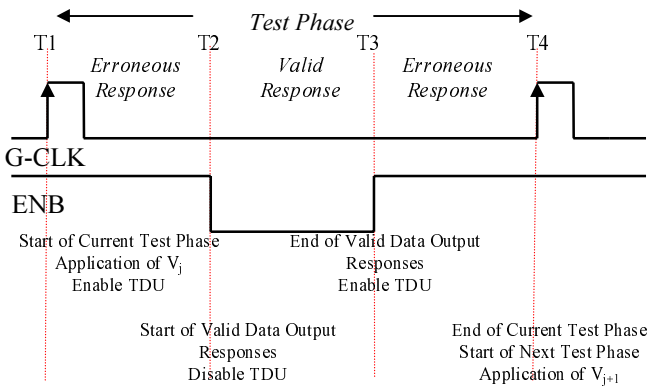

Figure 2. Timing waveforms