A Memory Architecure with 4-Address Configurations for Video Signal Processing

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Abstract

A memory architecture with four address configurations is proposed for video signal processing. The implemented 8-words X 64-bits 8-port SRAM has 256-bit simultaneous data accessability by horizontal and vertical address configurations and has 25.6 Gbits/s of high bandwidth.[1]

Embedded memory logic requires high bandwidth memory to handle data parallelism of video signal processing. However, conventionally designed SRAM [1]-[2] does not provide multiple data at a time, which becomes a bottleneck. Thus, we propose an architecture of 8-port SRAM which provides wide 256-bit simultaneous data. Four address configurations are HA: S[8n+i],S[8n+4+i]; HT: S[8n+2i],S[8n+2i+1]; VA: S[32p+2n+8i],S[32p+2n+8i+1]; VT: S[2n+16i],S[2n+16i+1] where H= horizontal, V= vertical, A= adjacent, T= alternate; S[ ]=SRAM cell; n=0,1,2,...; i= 0,1,2,3; p=0,1. To realize four address configurations, an 8-port SRAM with 256-bit data bus is devised with four data configurations by 4:1 column multiplexer arrays as shown in Figure 1. When one of the $WLi[7:0]$ is enabled, an access transistor of the 8-port cell is turned on, which connects the cell storage data to one of the $BLi[7:0]$. Each SRAM cell data is connected to one of the four ports in each multiplexer, and one of four data is connected to the $DATABUSi[31:0]$. Maximum 8 word lines of the $WL7[7:0]$ to $WL0[7:0]$ can be enabled. Thus, eight 32-bit SRAM data with four address configurations can be accessed through the 256-bit data bus at a time. To evaluate the proposed architecture, a benchmark test has been performed targetting IDCT by interfacing the proposed memory with a programmable DSP. The single-instruction multiple-data (SIMD) type 4-depth vector instructions are generated such as $movsr$: load S[8n+(4)+i]; $movrs$: store S[8n+(4)+i]; $vmovsr$: load S[32p+(4)+n+8i]; $movrs2$: store S[8n+2i+(1)] where n=i= 0 to 3; p=0,1; (n)= excluding or including n. The instructions are executed on the proposed SRAM by using four address configurations. Total 24 clock cycles are needed for the 32-pixels (half of 8 x 8 block) of the 1-D IDCT by logic simulations as follows: ClockCycles(Read,Write) = 1($movsr$) + 2($movrs$) + 1($vmovsr$) x 4(columns) x 2($subs$ and $adds$) + 1($movrs2$) x 2($subs$ and $adds$) = 13; ClockCycles(Compute) = 4($subs$) + 1($adds$) + 3(ldi) x 2(columns) = 11, where instruction $subs$ = subtract and shift right, $adds$ = add and shift right, and ldi = load data immediatley. The proposed memory requires 52 clock cycles to perform 8 x 8 block IDCT, which shows 2.5 to 4.9 times higher performance compared to conventional transposition memories [1]-[2] in accessing SRAM. The proposed memory implemented with 0.65um CMOS technology has 25.6 Gbits/s of high bandwidth, and can be used as an effective temporal storage to provide wide data bandwidth in video signal processing.

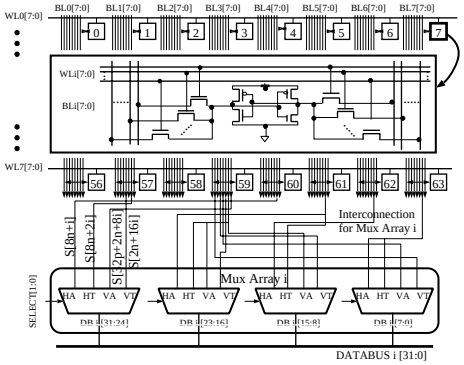

Figure 1. A memory architecture with 4-address configuraions

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References

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