Mixed-signal BIST using correlation and reconfigurable hardware*

J. Machado da Silva, J. S. Duarte, and J. S. Matos
University of Porto (FEUP) / INESC-Porto — Portugal
URL:dante.inescn.pt/cmel; jms@fe.up.pt

Abstract

Reducing the area overhead required by BIST structures can be achieved by reconfiguring existing hardware to perform test related control and processing functions. This work shows how the resources required for these operations can be implemented in-circuit, taking advantage of programmable logic available in the system. Structural and functional tests are performed using correlation to obtain i_{DD} and v_{OUT} cross-correlation signatures, and to measure gain, phase, and total harmonic distortion.

1. Discussion

In today's complex circuit assemblies (boards, MCMs, SOCs) different test methods are required to accommodate special needs of different functional blocks. Providing BIST support with low area overhead, over the entire product life-cycle, is of increasing importance. This is particularly true for mixed-signal circuits where both functional and structural tests may have to be combined to get a proper balance between test time, fault coverage, and performance characterization. This work addresses these issues taking advantage of the increasingly common situation where blocks of reconfigurable logic (FPGA) are available to implement system logic.

The circuit under test (CUT) consists of a data acquisition board containing a digital core and A/D and D/A interfaces together with the respective filters, which uses reconfigurable hardware to achieve a wide application range. Structural test of the analogue sections relies on evaluating the signatures obtained by cross-correlating power supply (i_{DD}) and output voltage (v_{OUT}) dynamic responses [1]. These correlations are performed in the FPGA using one bit quantisation of the signals — the so called polarity correlation. Functional testing is based on measuring the CUT's transfer function gain and phase using the correlation technique described in [2], that allows also total harmonic distortion (THD) measurements.

Figure 1 shows golden (dotted line) and faulty correlation signatures obtained for the DAC — the faults are *f3* a glitch in v_{OUT}, *f4* a 10% gain reduction, and *f7* a 50% degradation of the v_{OUT} signal to noise plus distortion ratio. Figure 2 shows golden (dotted line) and faulty correlation signatures obatained for a SC filter — the faults are *f5* a drift of Q from 8 to 5.6, and *f8* a halving of f_O and doubling of Q. Correlation performs also a compression of i_{DD} and v_{OUT} signatures — a single signature of 16×12 bit values is observed, instead of two responses comprising 4096×12 bit values each. Faults affecting i_{DD} are also detected. The gain and phase of the filter could be measured with an error of, respectively, 0.6% and 1.2%. Phase was measured with an error $< 5\%$ when performing polarity correlation. A THD of $-30dB$ (4 harmonics) was obtained for the DAC output voltage.

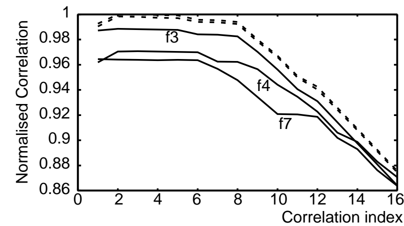

Figure 1. DAC i_{DD} -v_{OUT} correlation signatures.

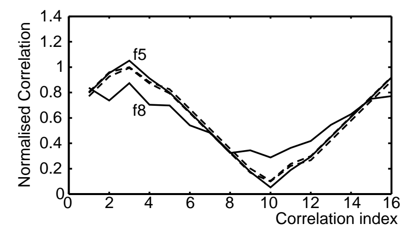

Figure 2. Filter i_{DD} -v_{OUT} correlation signatures.

The results presented herein suggest the effectiveness of testing by cross-correlating i_{DD} and v_{OUT}, even if low resolution observation is used. It is shown how reconfigurable system logic can be used to perform different structural and functional test operations and to provide in-circuit testability over the circuit's lyfe-cycle. These schemes can be used to test different functional cores, allowing thus for taking maximum advantage of existing resources.

References

[1] J. M. da Silva, J. S. Matos, I. M. Bell, and G. E. Taylor. Mixed current/voltage observation towards effective testing of analog and mixed-signal circuits. *Journal of Electronic Testing: Theory and Applications (JETTA)*, 9(1/2):75–88, August/October 1996. Special Issue on Analog and Mixed-Signal Testing.

[2] C. Elsden and A. J. Ley. A digital transfer function analyser based on pulse rate techniques. *Automatica*, 5:51, 1969.

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