# Cycle-Based Simulation Algorithms for Digital Systems Using High-Level Decision Diagrams

Adam Morawiec[1], Raimund Ubar[2], Jaan Raik[2]
[1] TIMA Laboratory, France; [2] Tallinn Technical University, Estonia

## Abstract

The paper addresses the problem of speeding up functional cycle-based simulation of digital systems. The system is represented as a network of interconnected Decision Diagrams (DD). Three new innovative simulation algorithms are introduced to implement the idea of simulation execution according to activities of the system variables: forward event-driven algorithm and two versions of back-tracing algorithms. Experiments are presented to show the simulation efficiency improvement offerred by those algorithms.

## 1. Introduction

It has been shown that the application of decision diagrams for the system representation and the cycle-based simulation of the DD-model offers a signifficant gain in the simulation speed in comparison to the event-driven HDL-based simulation approach [1]. The general objective of the presented work is to improve the simulation performance of the DD-based system representation by introducing the event-driven paradigm to the cycle-based simulation of the network of DDs.

## 2. Algorithms

DDs have been described in [1,2] as a representation of digital systems given at various levels of abstraction. DDs are used in the paper to increase the speed of local simulation of components or subcircuits of the system.

Three simulation algorithms are introduced to implement the idea of simulation execution according to activities of the system variables. In the first one, called *forward event-driven algorithm* (FED), before the evaluation of each diagram in the network, the input variables of the diagram are verified to check whether their values changed in the current simulation cycle in comparison to the previous one.

Other algorithms, called back-tracing algorithms, start to recursively evaluate the DDs of the network starting from the output variables. Two versions of the back-tracing algorithm are presented. In the first one the value of each output variable is calculated in every clock-cycle. In the second algorithm the output values are calculated only for the final clock-cycle of each simulation sequence.

## 3. Experimental results

Experiments were carried out on 5 benchmarks. In average, the forward event-driven algorithm offered the fastest performance with only 41 % of the number of diagram evaluations in comparison to the conventional 'compute-all' approach. The two backtracing approaches evaluated both about 58 % of the diagrams. Experiments showed that the efficiency of backtracing algorithms compared to the event-driven approach is dependent of the circuit structure. For the *gcd* circuit, backtracing algorithm, for other circuits, the event-driven approach were the fastest techniques.

The table presents run-times of the forward event-driven DD simulator and a commercial cycle-based HDL simulator Cyclone (Synopsys) on the five benchmarks. The number of variables and nodes in respective DD models are reported in columns 2 and 3 of the table. The experiment was run on 366 MHz SUN UltraSPARC 60. For optimal performance, Synopsys tools cylab and *cysim* were run with *-perf* and *-2state* options. As the table shows, DD event-driven cycle-based simulation tool offers the gain in simulation time between 2.5 and more than 14 times in comparison to the HDL simulator.

| Circuit | DD model | | Simulation time [s] | | Ratio |
|---|---|---|---|---|---|
| | # var. | # nodes | DD | HDL | HDL/DD |
| gcd | 15 | 34 | 0.20 | 0.51 | 2.55 |
| mult8x8 | 25 | 50 | 0.32 | 1.00 | 3.13 |
| diffeq | 37 | 57 | 0.25 | 1.26 | 5.04 |
| huff_enc | 61 | 161 | 0.34 | 1.40 | 4.12 |
| circ1 | 53 | 237 | 0.14 | 2.05 | 14.64 |

## References

[1] R. Ubar, A. Morawiec, J. Raik, “Cycle-based Simulation with Decision Diagrams”, Proc. DATE, pp 454-458, 1999.
[2] R.Ubar, “Test Synthesis with Alternative Graphs.”, IEEE Design&Test of Computers, pp 48-57, Spring 1996.
[3] P. McGeer, et al.: “Fast Discrete Function Evaluation Using Decision Diagrams”, ICCAD, pp 402-407, 1995.
[4] Y. Luo, T. Wongsonegoro, A. Aziz: “Hybrid Techniques for Fast Functional Simulation”, DAC, 1998.
[5] R. French, et al.: “A General Method for Compiling Event-Driven Simulation”, Proc. DAC Conf., 1995.