Cycle-true simulation of the ST10 microcontroller

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Abstract

With the rising complexity of electronic systems, containing more and more both hardware and software parts, it becomes necessary to simulate simultaneously hardware and software parts at whatever abstraction level. These simulation techniques, called co-simulation, require fast and flexible simulators. In this paper, we introduce the elaboration of a microcontroller simulator for an accurate hardware/software co-simulation at the clock-cycle level. It is our goal to have a simulator which is fast enough to simulate a few minutes of real time execution within a reasonable laps of time. To be more precise, we deal here with the realization of a simulator for the ST10 microcontroller and its integration into a co-simulation environment.

1. Introduction

It is our objective to study a working method for the development of microcontroller simulators which are precise at the cycle level and faster than the usual HDL-based simulation.

Our approach is a tradeoff solution between the instruction set simulator and the HDL model: we designed a microcontroller model, that simulates the whole circuit including the peripheral at the clock cycle level.

We wrote a model of the ST10 which is manufactured by STMicroelectronics, and is composed of a 16-bit pipe-lined processor and a set of peripherals (ADC, serial interfaces, etc.).

2. The ST10 simulator

The ST10 simulator is composed of 3 parts : a first part that simulates the core, another one that simulates the peripherals, and finally a main loop in charge of activating the core and the peripherals at each cycle.

2.1. The model of the core

The model of the core has been designed by means of Flexsim, a generator of sequential instruction set simulators developed by STMicroelectronics. This program is actually a kind of compiler that takes as input a description of the processor in a language called IDL and produces as output the C code of the simulator.

2.2. Peripheral models

The model of the peripherals has been designed in C. Those components are usually composed of two parts : a control part which is an automaton, and an operative part which is a set of registers, computing parts and analog parts. The simulation of the first part was done by a C switch/case structure on a variable that represents the state. the simulation of the second part was done by reproducing its behavior in C.

3. Result, evaluation and future works

The final simulator can run at a speed between 30,000 and 50,000 instructions /second on an Ultra Sparc station of 167 MHz having it run without traces. It has been integrated into a co-simulation environment, and used for simulation with several software and hardware parts.

Although the simulator is faster than the software HDL simulators, we noticed that some operations computed by the simulator were often useless. Moreover, it might be overdoing it a little bit when reproducing the internal architecture just for the simulation purpose. In fact we found two main sources for optimization: the pipeline simulation and the flag management. The first ignores some details of the architecture in order to simplify the simulator. The second reduces the number of useless computations made by the simulator.