Evaluation of Interconnects with TDR

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Abstract

In this paper, a novel technique is presented for the verification of board level connections on PCBs. The time domain reflectometry (TDR) method is used to identify whether a pin connection is faulty or not. The test pulse - and evaluation circuitry is part of the chip. Although the chip size increases slightly, the method is highly efficient. No Automatic Test Equipment (ATE) is necessary to carry out the test and since only the physical behaviour of the connection from the internal driver via pin to board is examined, no test vectors are needed. The test time and the test preparation time are lower compared with conventional test methods.

Introduction

The proposed method is intended for total selftest applications without external test equipment. Common test approaches compare testpatterns on the send and receive side and require thus a substantial amount of memory, circuit logic and computer power. With this method, the test result can be determined immediately after the test. The test circuitry can be minimized to chip level size and is ideal for a selftest strategy.

Test Principle

The connection under test is considered as a transmission line and has to be stimulated such, that the response can be evaluated and accessed on the internal test observation circuit (Fig.: 1).

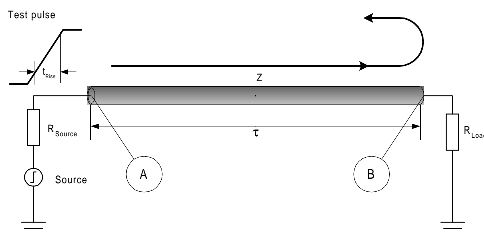

Figure 1 Transmission Line Model

The size of the reflected wave depends on more parameters [1, 3], but R_{Load} can be extracted (1). On exactly 2τ the result must be read out. Response waves after 2τ are caused by terminations on board and thus not considered further. R_{Load} as a representation of the quality of the pad can be calculated as:

$$R_{Load} = Z_0 \cdot \frac{V_{2\tau} - V_A + V_0}{V_0 - V_{2\tau} - V_A} \quad (1)$$

Results

Testresults from a typical PLCC package are shown in Fig.2. It can be seen, that at V_A=0.6 V the connection is considered fault free.

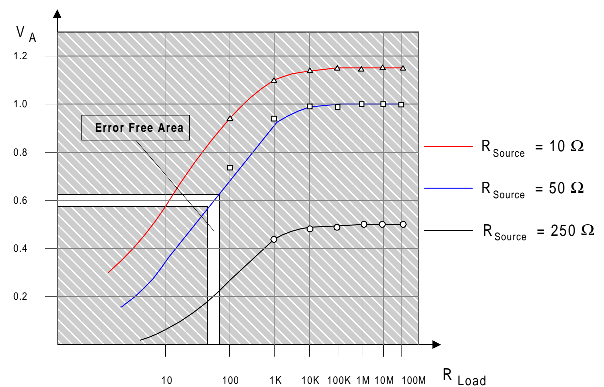

Figure 2 Test results for a PLCC package

Conclusion

A new technique to test solder connections from pin to board has been presented. Experiments attest the accuracy of the method compared with calculated data.

Since this is a radically new technique for testing interconnects the trade-off between test coverage / test accuracy and test cost / chip space can be optimized. Further investigations aim to reduce the required chip space and if the technique is transferred into a general model its application to different packages and chip families becomes possible.

References

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