XFridge: A SPICE-based, portable, user-friendly cell-level sizing tool

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Abstract*

This paper presents a user-friendly tool which allows automated sizing of IC cells. It comprises an open optimization-based sizing program, a database which allows knowledge re-use and also easy addition of new knowledge, and a powerful graphical user interface.

Tool description

The increasing demand of analog circuits in mixed-signal ASICs constitutes a challenge for today's IC designers. This is mainly due to the need to produce high performance analog blocks in adverse digital technologies at the vertiginous rate imposed by the technology and market evolution. This has motivated the interest for supplying CAD tools which can assist the design procedure.

Focusing our attention on the lowest level of the design hierarchy, design automation of building blocks has been a recursive topic in literature [1]-[3]. Among the different possibilities, it is now accepted that combining optimization and electrical simulation is one of the best approaches because viability of the sized cells is guaranteed. Our work in this approach resulted in FRIDGE, an open tool for sizing basic cells of ICs which combines heuristic modifications of the simulated annealing algorithm with a design-oriented formulation of the cost function to solve the sizing problem within reasonable CPU times [4].

XFridge is intended for offering a robust framework which compiles the previous experience, and is composed of three main modules: (a) cell-level sizing tool FRIDGE; (b) knowledge library which manages accumulated design experience; and (c) graphical user interface.

The knowledge library addresses the re-use of the large amount of knowledge generated with the repetitive use of FRIDGE, which was not easily re-usable from one execution to another, or from one user to another. It is composed of a library database and a library manager which contain previous netlists, suitable configurations to measure performances, proper design constraints, previously sizings a good starting points for new designs, proper settings of algorithm parameters, etc.

User friendliness has been addressed by the incorporation of a graphical user interface based in TCL-TK language aimed to easily input required information to FRIDGE, monitor the design procedure, collect results, collect information from the knowledge library and pass it to the user and to FRIDGE, transmit knowledge to the library.

As an illustrative example, the fully-differential folded-cascode OTA in Fig.1 has been sized in a 3.3-V 0.35µm CMOS technology with the specifications in Table 1. The sizing was performed

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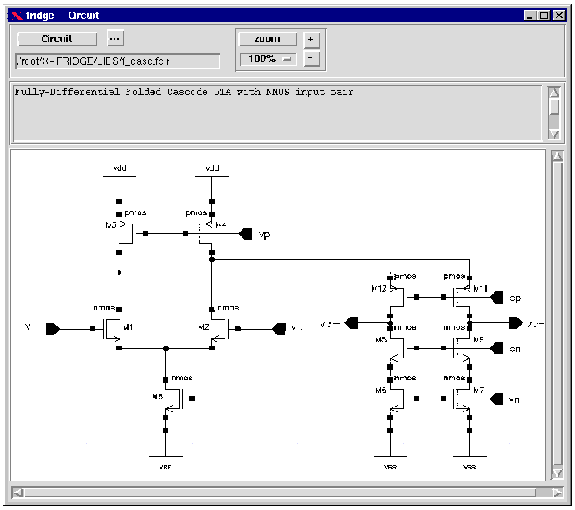

Figure 1. Example of a cell schematic in Xfridge.

starting from an arbitrary point in a wide design space. For instance, transistor widths were allowed to vary in the range [2µm, 800µm]. The electrical simulator used was SPICE3 [5]. Table 1 shows the cell performance obtained after 4min. CPU-time in a 200-MHz PC.

References

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Table 1: Performances for the OTA (2pF/branch)

	Specified	Xfridge
DC-gain	60dB	60dB
GB (MHz)	300	300
PM (Degree)	60	67.3
Inp. noise at 1kHz / 10MHz	200 / 5 (nV/ $\sqrt{\text{Hz}}$)	186/4.3 (nV/ $\sqrt{\text{Hz}}$)
SR (V/µs)	250	317
OS (V)	± 2.0	± 2.0
Power (mW)	minimum	4.45
Channel area	minimum	29x29µm^2