

Area Optimization of Analog Circuits Considering Matching Constraints

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Abstract

A new, fully analytical method is presented to optimize active device area in complex, device mismatch sensitive analog circuits. It represents an efficient alternative to time consuming Monte-Carlo simulations and numerical iteration procedures for design centering.

1. Introduction

In precision analog circuits, often pairs of devices or exactly weighted devices are used, which are required to match, i. e., to show equal electrical parameters. Due to random effects during processing and due to fabrication tolerances, parameter variations between these devices occur.

Usually the mismatch-induced standard deviation of relevant electrical CMOS device parameters is proportional to $1/\sqrt{A}$, where A is the active device area. For transistors and resistors, mismatch of their most important parameters can be described using the relations [1–3]:

$$\sigma_{\Delta V_t} = \frac{c_{\Delta V_t}}{\sqrt{A}}, \quad \sigma_{\Delta k/k} = \frac{c_{\Delta k/k}}{\sqrt{A}}, \quad \text{and} \quad \sigma_{\Delta R/R} = \frac{c_{\Delta R/R}}{\sqrt{A}}. \quad (1)$$

V_t is the transistor threshold voltage, k the transistor constant, R the resistance of the resistor, and $c_{\Delta V_t}$, $c_{\Delta k/k}$, and $c_{\Delta R/R}$ are the related matching constants.

2. Area Minimization

Device mismatch leads to small deviations of the output signal. Assuming uncorrelated device parameters p_{ij} , the total standard deviation of the circuit's output signal $S_{\text{out}} = f(S_{\text{in}}, p_{11}, \dots, p_{mn})$ is calculated following the Gaussian approach:

$$\sigma_{\text{out}}^2 = \sum_{i=1}^m \sum_{j=1}^n \left(\frac{\partial S_{\text{out}}}{\partial p_{ij}} \right)^2 \frac{c_{ij}^2}{A_i}. \quad (2)$$

There, the parameters c_{ij} are the matching constants related to the examined parameter j of device i .

By varying area A_1 of a fictive two-parameter system, its total area A_{tot} is calculated on the basis of eq. (2) for two given values of σ_{out} (Fig. 1). This simple example clearly demonstrates that a narrow optimum area configuration exists. Thus, a method to properly weight device areas in real circuits is demanded, where a complex multidimensional system must be considered.

Eq. (2) is the boundary condition of the optimization procedure concerning the sum of device areas A_i . To find the minimum of $A_{\text{tot}} = \sum_i A_i$, the Lagrange formalism is used.

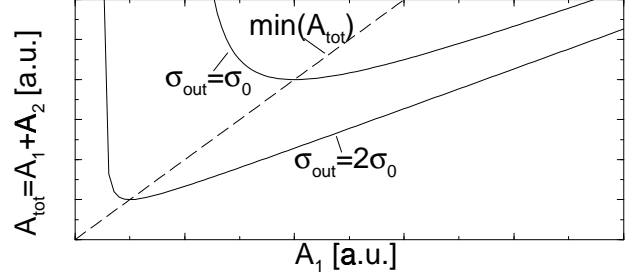


Figure 1. Area amount of a two-parameter system for two given values of the maximally allowed standard deviation σ_{out} (eq. (2)). The dashed line indicates the optimum area configuration.

In this case, the Lagrange function \mathcal{L} is given by:

$$\mathcal{L} = \sum_{i=1}^m A_i + \lambda \left(\sigma_{\text{out}}^2 - \sum_{i=1}^m \sum_{j=1}^n \left(\frac{\partial S_{\text{out}}}{\partial p_{ij}} \right)^2 \frac{c_{ij}^2}{A_i} \right). \quad (3)$$

The formalism leads to a minimum value for the device areas:

$$A_i = \frac{\sum_{i=1}^m \sqrt{\sum_{j=1}^n \frac{\partial S_{\text{out}}^2}{\partial p_{ij}} c_{ij}^2}}{\sigma_{\text{out}}^2} \sqrt{\sum_{j=1}^n \frac{\partial S_{\text{out}}^2}{\partial p_{ij}} c_{ij}^2}. \quad (4)$$

These analytically derived equations allow to calculate the optimum area for each device within a considered circuit. To evaluate the device areas only the derivatives of the transfer function S_{out} of the circuit and the matching constants of the devices used are needed. While the matching constants for the process used have to be determined experimentally, the derivatives of the transfer function can be obtained on the basis of a sensitivity analysis which is a standard tool in circuit simulation environments.

3. System optimization

For the design of large systems usually sub-circuits are considered. Note, that without a loss of performance, also the area optimization of the whole system can be performed by applying the proposed method to a given set of sub-circuits. In analogy to the formal structure of eq. (1) new matching constants related to these sub-circuits are defined and used in eq. (2) instead of single device related matching constants. This procedure allows a strictly organized hierarchical area optimization.

[1] K. R. Lakshmikummar et al.. *IEEE JSSC*, p. 1057ff, Dec 1996.

[2] J. Bastos et al.. *Proc. ICMTS*, Vol. 8, p. 271ff, Mar 1995.

[3] R. Thewes et al.. *Tech. Dig. IEDM*, p. 771ff, 1998.