Designing Closer to the Edge

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Abstract

Modern deep submicron CMOS processes cost $2B or more to develop, qualify and deploy. Yet the incremental impact of each technology generation has been steadily decreasing due to a variety of phenomena such as increasing wire delay, power dissipation and reliability limits, and increasing process tolerances. This increase is portrayed in Figure 1 which shows the SIA Roadmap[1] predictions of variability for five technologies in the 250 to 70nm gate length regime. These observations lead to the conclusion that we need to make better use of existing and future manufacturing processes in order to recoup our investment.

When using of an existing process, the designer get the dual benefits of low cost and process maturity at the cost of (a) lower performance and (b) lower integration density. While the lower integration density is somewhat unavoidable, it is often possible to get more performance out of an existing technology by better understanding of the process tolerances and trading off functional yield vs. performance.

Given the above, it is clear that we need to understand and model design tolerances arising from processing variations. Until recently, it was sufficient to model such process-induced variations as intra-die shifts in device performance. However, in the deep sub-micron regime, within-die wire and device variations are comparable to die-to-die variations. This results in the need for new characterization, modeling and analysis techniques to handle these variations.

To re-enforce these ideas, consider the simple canonical circuit in figure 2 composed of a source buffer driving an identical destination buffer through a length of minimum-width wire. We examine the relative impact of wire and device variability on the delay for various technology generations. Across technologies we maintained the W/L ratio for the buffer and found the maximum wire length beyond which inserting a buffer between the source and destination would lower overall delay[2]: $L_{max} = \sqrt{2(\tau_B + R_B C_B)/R_w C_w}$, where τ_B, R_B and C_B are the delay, output resistance and input capacitance of the buffer, and R_w and C_w are per unit length of the wire.

Taking the same five technologies in figure 1 and computing L_{max}. The results are shown in table 1 and figure 2 which explains the wire geometrical parameters. The table shows a super-linear (relative to L_{eff}) decrease in the length L_{max} vs. process generation, which shows and increase in the influence of interconnect. When we extend the analysis to include the impact of the device and wire variations on the delay variations we see that the contributions of of device and wire variability to total delay variability remain fairly constant (table 2) which is important because it means that this canonical circuit is a good gauge to differentiate circuits based on their sensitivity to device and wire variations. If we do the analysis without scaling transistor widths (case (A) in table 2), or scaling wire length at the same rate as L_{eff} (case (B) in table 2) we get very different results.

In this tutorial we will expand on the ideas above, review the important trends in design uncertainty which directly drives design tolerance and hence performance. We will review a number of research and applied approaches to design for manufacturability. The need to track process tolerances as a technology matures will be stressed. This tracking is important since it acts as an information conduit between design and fabrication groups and enables designers to adapt the design to lower tolerances where possible.

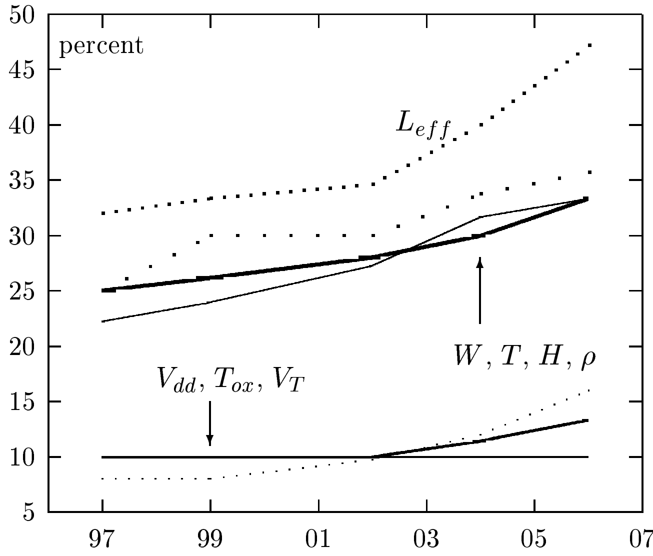

Figure 1: Technology parameter variations.

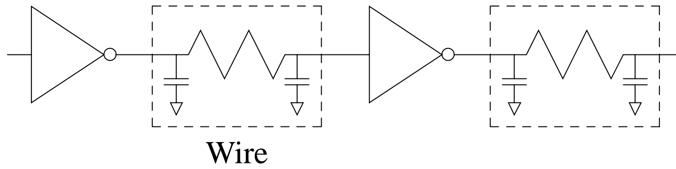

Figure 2: Canonical circuit.

	1997	1999	2002	2005	2006
L_{eff} (nm)	250	180	130	100	70
T_{ox} (nm)	5	4.5	4	3.5	3
V_{dd} (V)	2.5	1.8	1.5	1.2	0.9
V_T (V)	0.5	0.45	0.4	0.35	0.3
W (μ)	0.8	0.65	0.5	0.4	0.3
H (μ)	1.2	1.0	0.9	0.8	0.7
ρ ($\frac{m\Omega}{\Box}$)	45	50	55	60	75
L_{max} (μ)	*2123*	*1920*	*1670*	*1526*	*1303*

Table 1: Technology parameters.

	1997	1999	2002	2005	2006
Constant W/L, wire length = L_{max}					
Device (%)	47	47	44	44	45
Wire (%)	53	53	56	56	54
Case (A): no scaling of device width					
Device (%)	47	43	37	35	34
Wire (%)	53	57	63	65	66
Case (B): scale wire length with L_{eff}					
Device (%)	47	51	52	55	60
Wire (%)	53	49	48	45	40

Table 2: Device and wire contribution to delay variations.

References

[1] *The National Technology Roadmap for Semiconductors*, 1997.

[2] C. Alpert, A. Devghan, and S. Quay. Buffer insertion with accurate models for gate and interconnect delay. In *Proceedings of DAC*, 1999.