# A VHDL-based Methodology for the Design and Verification of Pipeline A/D Converters

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**Abstract**

*This paper proposes a methodology for designing sampled-data Mixed-Signal circuits by using VHDL-based behavioural descriptions. The goal is using a VHDL description of both the analog and the digital part, to simulate and verify the entire mixed-signal system, as well as to facilitate the synthesis and fault simulation of the digital part. As an example of the proposed methodology, a digitally corrected/calibrated pipeline A/D converter (ADC) has been designed. Among other aspects of general interest, we will show how analog dynamic effects are incorporated in order to obtain accurate high level simulations. Results from simulations carried out using QuickHDL in Mentor-Graphics prove the feasibility of the approach and are in agreement with those obtained experimentally from a Silicon prototype.*

## 1. Introduction

VHDL descriptions are widely used for digital circuits synthesis and verification. For complex mixed-signal ICs there is also the need of system-level design and simulation, and thus efforts are currently under way to define and implement an extension of VHDL towards analog languages [1]. Until this standard comes up, the development of analog models suitable for VHDL description is a challenging issue [1,2,4]. Evidently, the implementation of an analog behavioural model that is deeply related to the logical description of a digital system is possible in mixed-mode simulators as Saber, Eldo, Spectre-Verilog, Smash, etc. However, in some of these cases the automatic synthesis of the digital part requires a translation of the digital description from the mixed-mode simulator to VHDL. For mixed-signal systems with a digital part of high complexity, it seems more appropriate to describe the behavioural model (analog and digital) directly in VHDL and to synthesize the digital part using the required digital resources.

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In this paper we will show how VHDL can be efficiently used to simulate and verify the functionality of digitally corrected/calibrated pipeline ADCs. Having achieved this, the digital part of the VHDL may be synthesized with a high confidence in that the entire system will operate as intended. In addition, analysing the fault coverage of this part is facilitated, and the basis for a solution to test program generation is provided.

Our motivation originates from the need of synthesizing the digital part of the pipeline ADC with enhanced testability proposed in [3]. The complexity of the digital circuit derives, in this case, from the incorporation of correction, calibration, and control of different testing modes. Verifying all the operation modes of the system in an early phase of design and having the possibility to quickly perform modifications (or to prove alternative calibration algorithms) leads us to develop the VHDL-based behavioural model of the whole system. This model must be simple but at the same time sufficiently precise and detailed to be able to predict static and dynamic performance.

There exists other additional incentives making particularly interesting the VHDL description of the analog part in this converter design. One of them derives from the requirement of an exhaustive set of realistic patterns coming from the analog part and needed to verify the digital part. Although these patterns can be separately obtained with other software tool, in some modes of operation, as for instance under digital calibration, the generation of input patterns for the digital subsystem is intimately dependent of the control that the digital part has on the analog part. These situations where a feedback loop exists between the digital and analog processes are difficult to verify using separate simulation tools.

A summary of the proposed methodology is depicted in Fig. 1.

The paper is organized as follows. Section 2 presents how the VHDL-based model is implemented, and Section 3 explains its application to an ADC example. Simulation and experimental results are illustrated in Section 4. Finally, Section 5 gives the main conclusions.

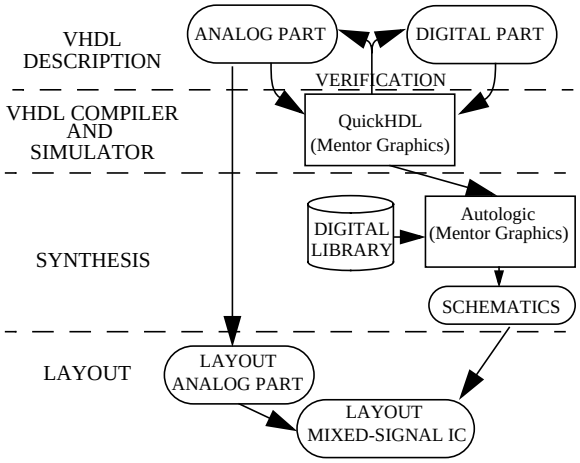


Fig. 1 Proposed design methodology.

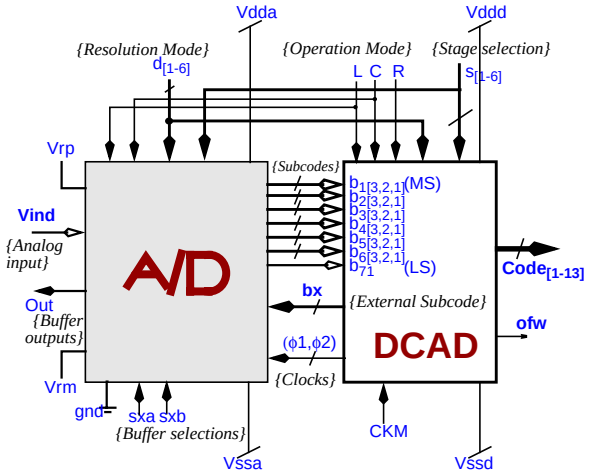


Fig. 2 Structural representation of the VHDL hierarchy

## 2. The VHDL-based converter model

The basic structural VHDL subdivision carried out among the analog part and the digital part of the system is illustrated in Fig. 2. The two blocks in the highest level of the hierarchy are shown. The block labelled A/D represents the analog part of the converter. The modelling of their behaviour is an important part of the work presented here. The block labelled DCAD represents the digital part of the converter, that will be synthesized from VHDL. It controls all the operation modes of the block A/D and processes its outputs (subcodes). This block has been modelled following an RTL description of its operation, being fully synthesizable for the silicon compiler used.

The hierarchical structure given to the A/D block for VHDL description purpose is shown in Fig. 3. The blocks identified as *SH*, $STG_i$, and the $A/D_k$ are the basic entities of description which are modelled in a functional way; they represent the sample&hold, the converter analog stages, and the last quantizer, respectively. The developed models include [4]: (i) static errors of linearity, gain and offset, and, (ii) dynamic errors mainly due to local settling errors. The parameters for defining the behavioural model were obtained from both the general specifications of the system and the physical parameters of the circuits used in the integration of the prototype in [3].

Analog modelling using HDL event-driven descriptions requires defining sampling points at which the model produces new values based on its inputs and internal state [5]. The sampling points should be defined by the clock controlling the event-driven simulation. Pipeline converters work with two clock phases; a stage $STG_i$ takes a new input value during the same phase the output of the preceding stage $STG_{i-1}$ is validated. For correct simulation of these situations where two events occur simultaneously, a proper or-

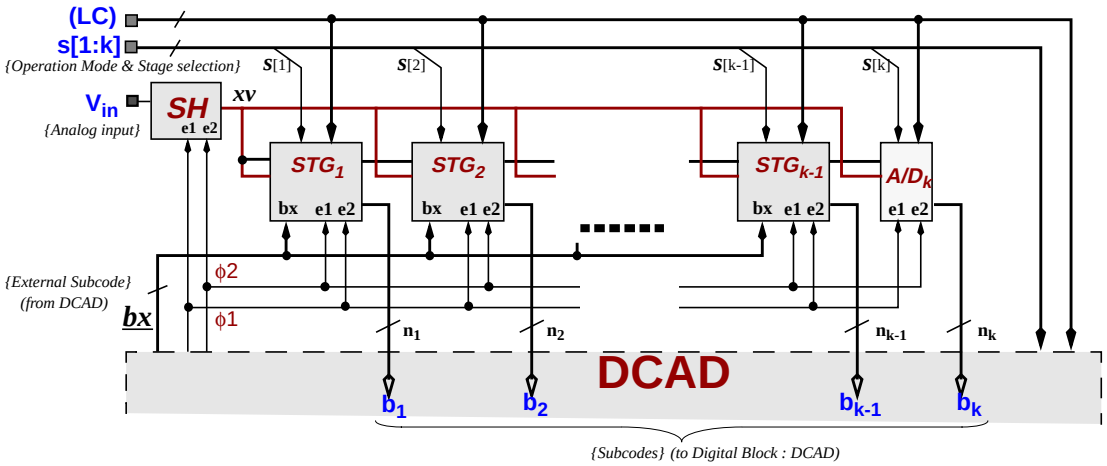


Fig. 3 Structural representation of the A/D block in Fig. 2

dering in the priority of events is required. For our model, we have adopted the approach illustrated in Fig. 4. On this basis, the HDL description for the functional operation of the $STG_i$ cells in Fig. 3 is as shown in Fig. 5.

Figure 6 depicts the hierarchical structure given to the DCAD block. This block operates with one master clock (CkM) that generates three different phases: ϕ1 and ϕ2 are used for loading data from the A/D, and Ckb is used for computation. The main entities consist in: an array of shift-registers (SHR) intended for synchronization of subcodes, a correcting logic array in a ripple carry configuration (CfR), some arithmetic logic for calculating and averaging calibration errors, a set of register-bench for storing the error codes, a sequential block for generating external subcode (bx) used for testing and calibration purposes, and glue logic for selecting modes and generating internal control signals.

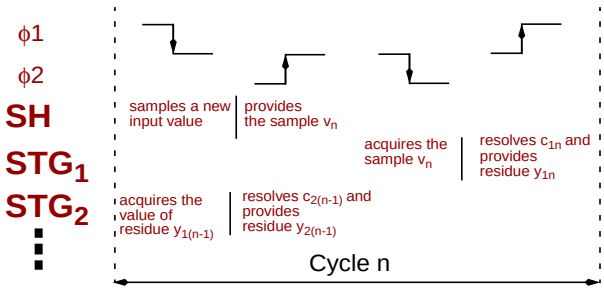


Fig. 4 Ordering of events and corresponding operations set for the A/D block

## 3. Design example

The proposed methodology has been applied for synthesizing the digital part of the testable pipeline ADC reported in [3], as well as for simulating the whole system. This demonstrator is a 10-bit of accuracy, 10MSamples/s ADC composed of 6 stages, each of one being programmable for 2 or 3 bits of resolution, one of them is always used for digital correction. Thus, the output code has a maximum of 13 bits. The photograph of a CMOS fully-differential switched-capacitor (SC) implementation in a 1.2µm process is depicted in Fig. 7a. For the experimental characterization of this prototype digital calibration and correction were off-chip executed [3].

The synthesis of the digital part has been now obtained using the methodology presented in this paper. The resulting chip (Fig. 7b) occupies 1.84mm$^2$ (without pads) in a 0.6µm CMOS technology. CAD tools used were QuickHDL and Autologic from Mentor Graphics for VHDL simulation and logic synthesis, respectively. The effort estimated for this design was 1man/month for description and verification, while the synthesis process takes only one

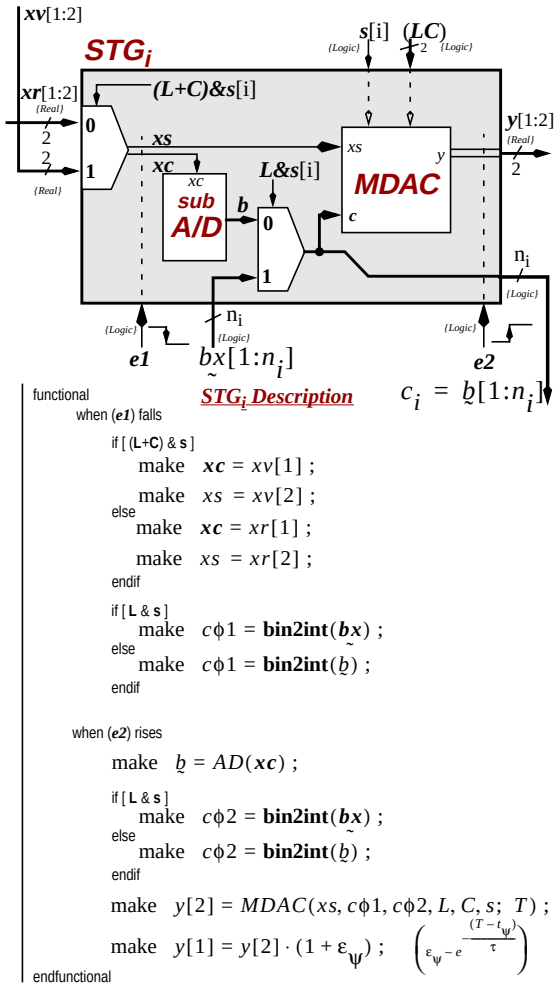


Fig. 5 HDL description for the $STG_i$ entity in A/D block

day, once the exact and precise VHDL description is reached.

## 4. Experimental results

Simulation and experimental results for the whole system are depicted in Figures 8 and 9. In Fig. 8(a) the Effective Number of Bits (ENOB) given by VHDL simulations is shown as a function of the sampling frequency for three different cases: without calibration, and with two different types of calibrations. Fig. 8(b) shows the ENOB given by VHDL simulation as a function of the input signal frequency for the same three cases and without the use of additional SH at the input. It can be seen how the lack of the input SH stage worsens the resolution of the ADC at frequencies higher than 800 kHz in the simulated case. These results show the suitability of the VHDL model for representing

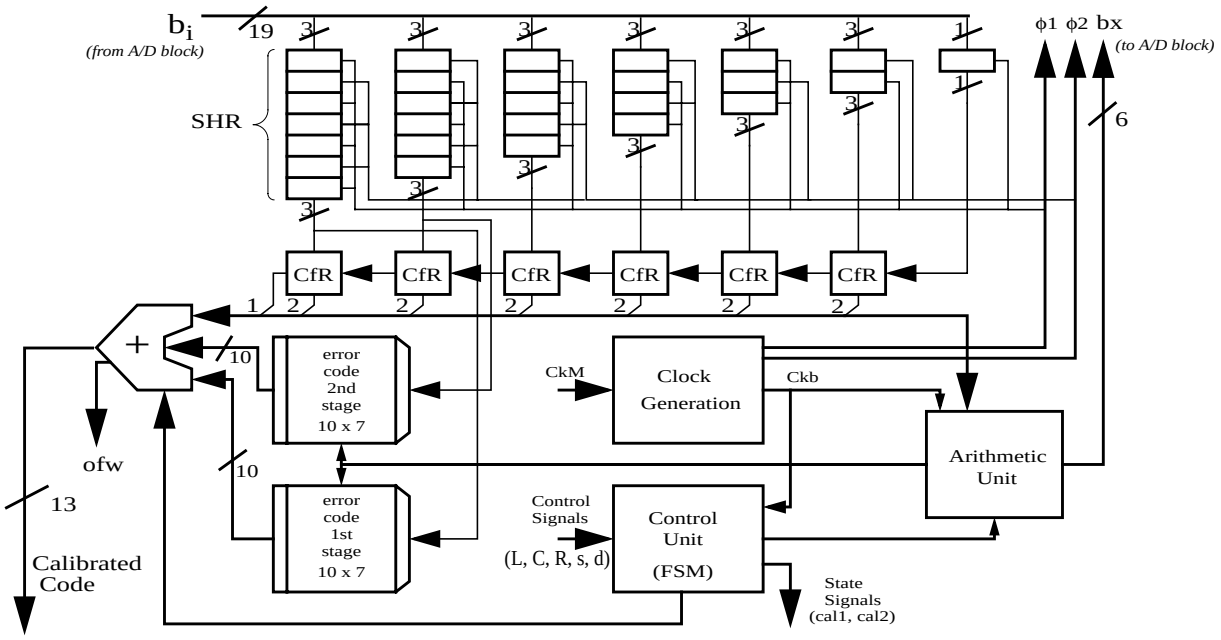


Fig. 6 Hierarchical structure of the DCAD block in Fig. 2

the dynamic expected behaviour. On the other hand, Fig. 9 shows the Integral Non-Linearity (INL) obtained both experimentally in the lab from the Si prototype and from the VHDL model, for the case of first and second stages calibrated and without interstage-gain calibration. As it is shown, there is a good correspondence between both representations.

As was previously mentioned, the availability of a VHDL description of a mixed-signal system makes easy fault coverage analysis. Stimuli patterns for the fault simulation of the digital circuitry can be derived for every operation mode of the analog part, hence, testing techniques and optimal test program could be developed. We are going on with the work in that direction. At this time, some results has been obtained for the pipeline ADC demonstrator; for example, Verifault-XL simulations of the digital circuit using test patterns derived during the calibration of the two first stages and for ten analog input levels, gave 59.3% of fault coverage.

## 5. Conclusions

A methodology for using VHDL description to simulate and verify digitally event-driven mixed-signal systems has been explored. As an example of design, a corrected/calibrated pipeline A/D Converter has been considered. VHDL-based behavioural models for the analog part of the circuit have been proposed and validated through extensive QuickHDL simulations of the complete ADC. The digital part of a testable ADC including many different modes of operation has been automatically synthesised from its VHDL description. Stimuli patterns for the fault simulation of the digital circuitry can be derived for every operation mode of the analog part, thus allowing fault coverage analysis. Some experimental results proved the suitability of the proposed approach. Although a pipeline ADC has served as demonstrator of the methodology, our experience allows us to conclude that it could be applied to other mixed-signal circuit if proper models are developed for the analog circuitry.

## 6. References


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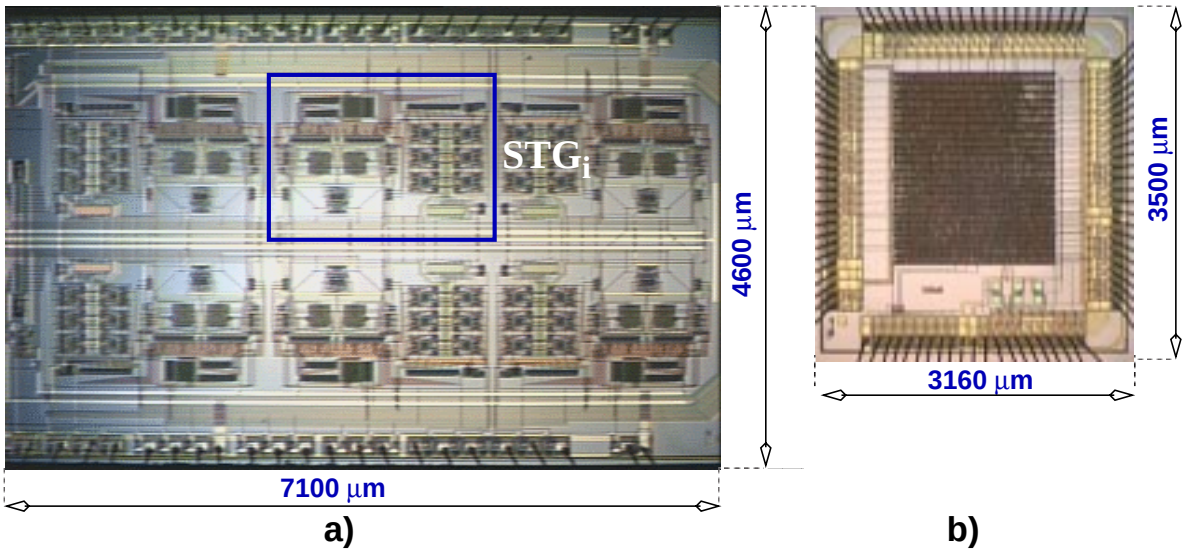


Fig. 7 Microphotograph of the a) analog and b) digital part of the ADC

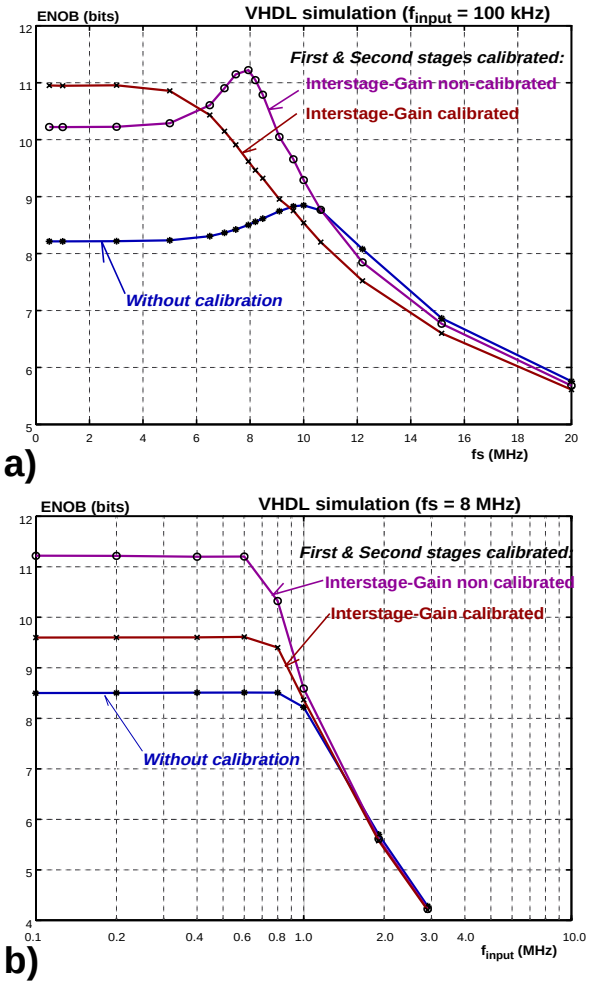


Fig. 8 Dynamic results from VHDL simulations

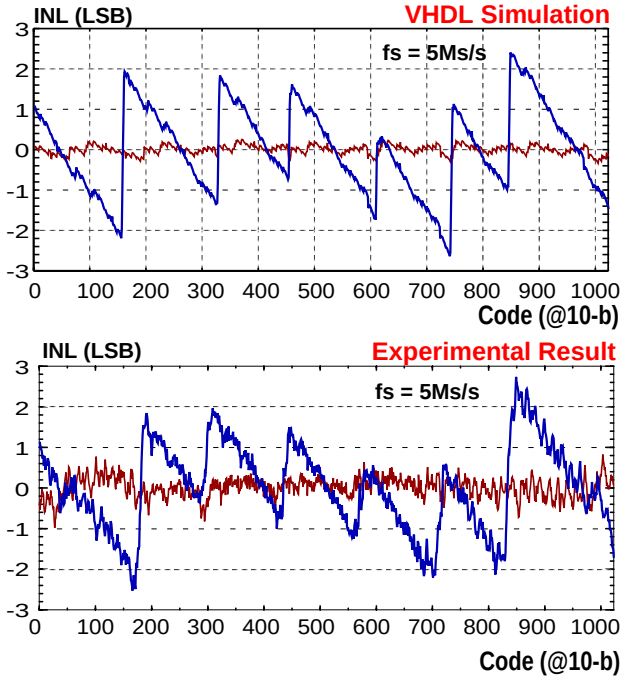


Fig. 9 Static results from VHDL simulations (top) and from the silicon prototype (bottom)