# All Digital Built-in Delay and Crosstalk Measurement for On-Chip Buses

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## Abstract

*This paper proposes an all digital on-chip bus delay and crosstalk measurement methodology. A diagnosis procedure is derived to distinguish the delay faults in drivers, receivers, and wires. The crosstalk profile is plotted by monitoring the changes in delay with the presence of the crosstalk. The distinguished features include all digital design and low hardware overhead. The SPICE simulation results prove the feasibility of the methodology.*

## 1 Introduction

The delay and crosstalk of on-chip bus is a critical design and implementation consideration for deep submicron integrated circuits [1, 2, 3, 4]. The bus delay is a decisive factor in determining the circuit performance and the crosstalk raises a reliability concern. Not only the design and implementation of the bus but also its testing and diagnosis are the emerging issues in the deep submicron era.

The bus delay is the result of (1) insufficient driving capability of the driver, (2) too much stray resistance, capacitance, and inductance of the wire, and (3) insufficient gain of the receiver. If the delay exceeds a clock period, the system will definitely fail. However, if it does not, the extra delay shortens the design margin and raises a reliability concern. Similarly, the crosstalk incurs noise in adjacent channels. In addition to the shortened noise margin, it also creates a timing uncertainty (jitter) in the signal. As a result, the delay and crosstalk measurement is needed to know the cause to improve the yield and the reliability.

The measurement of on-chip delay and crosstalk is not an easy task. The added probing pads and external probing create more stray capacitance than that of the bus, not mention that the probing is time consuming and requires very expensive instrument. In [3], a novel electron-beam prober with 15ps time resolution is used to measure the clock signal. Although no special pad or test structure were required, however, the solder balls and the passivation must be removed. In [4], a dedicated test chip has been implemented to measure the delay and crosstalk for the calibration of the TCAD tools. Considering the cost and the effort, a built-in module to aid the measurement is desirable.

Here, an on-chip bus delay and crosstalk measurement methodology is proposed. It has the following distinguished features. First, it measures the delay of the bus and locates the fault site. Second, it retrieves the crosstalk effects by the delay measurement. Third, the metrology is accomplished in digital means. Therefore, it is technology independent and easily portable.

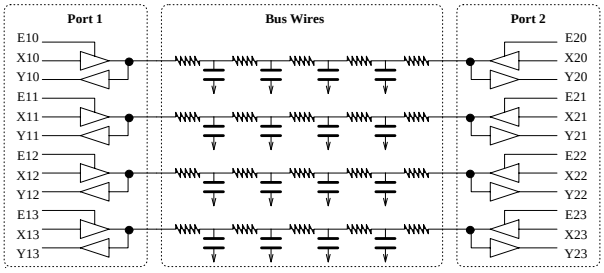

Figure 1: The bus model.

In the rest of this paper, the discussion proceeds as follows. In Section 2, the bus and fault models are presented. In Section 3, the digital delay measurement technique is studied. In Section 4, the delay measurement architecture is detailed. In Section 5, the diagnosis configurations are outlined. In Section 6, the theories and the design of the crosstalk measurement are illustrated. In Section 7, the test results are presented to reassert the methodology. Finally, in Section 8, the conclusions are given.

## 2 Bus Model and Fault Model

A simplified circuit level model of buses is shown in Figure 1. Here, the stray resistance (R) and capacitance (C) of the wires are shown. The adjancent-wire coupling capacitance is considered but not shown in the figure. Two major fault categories are under consideration, the bus delay fault and the bus crosstalk fault. The *bus delay fault* is referred to the extra signal delay of the bus. The bus delay faults are further divided into three subclasses, the *driver delay faults*, the *receiver delay faults*, and the *wire delay faults*. The *bus crosstalk fault* is referred to the case when the noise coupled from adjacent wires is so large that the data polarity and timing are significantly affected.

## 3 Digital Delay Measurement

For the timing measurement, a conventional *time-to-digital converter* is shown in Figure 2 [8]. The phase between the two signals are detected by a *phase detector* (PD). It can be implemented by an exclusive OR (XOR) gate. The output of the PD is a square

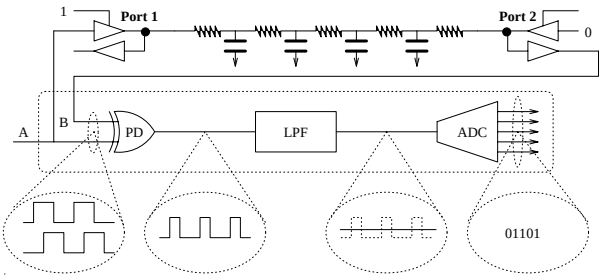

Figure 2: The analog phase measurement.

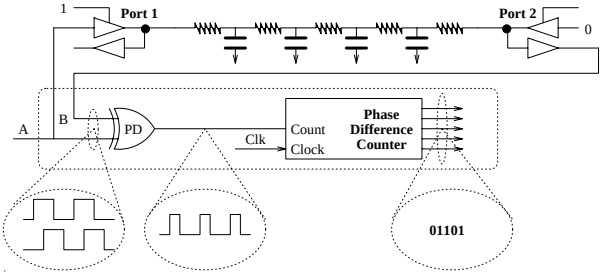

Figure 3: The digital delay measurement.

wave with a duty cycle proportional to the phase differences. Then, a lowpass filter (LPF)is used to remove the high frequency components and obtains a DC value that representing the phase differences. To obtain a digital readout, one can use an *analog-to-digital converter* (ADC) for the conversion. The use of analog components, such as LPF and ADC, is a major disadvantage because it is technology dependent. Hence, a technology independent digital design is desirable. The theoretical ground work for a digital delay measurement is discussed as follows.

As stated earlier, the output of the PD is a square wave with a duty cycle proportional to the phase difference. Suppose that the phase difference is $\phi$, then the duty cycle is $\phi/\pi$. If the PD output signal is randomly sampled $n$ times and $n$ is sufficently large, the outcome will have $k$ number of 1's. The relationship among $\phi$, $n$, and $k$ is as follows.

$$k = n \times \frac{\phi}{\pi}. \tag{1}$$

According to the above derivation, the digital delay measurement module is proposed in Figure 3. The phase difference signal $\phi(t)$ is sampled by an asynchronous clock Clk. If $\phi(t)$ is high at the edge of Clk, the *phase difference counter* PDC is increased by one. Suppose $k$ is the content of the PDC after $n$ samples, the delay can be calculated by Eq. (1). The most significant advantage of the proposed digital delay measurement is its pure digital design. This property makes the proposed technique easily portable. With such a digital delay measurement method, a bus delay measurement architecture is proposed as follows.

## 4 Bus Delay and Crosstalk Measurement Architecture

The proposed *Bus Delay and Crosstalk Measurement* (BDCM) architecture is shown in Figure 4. The

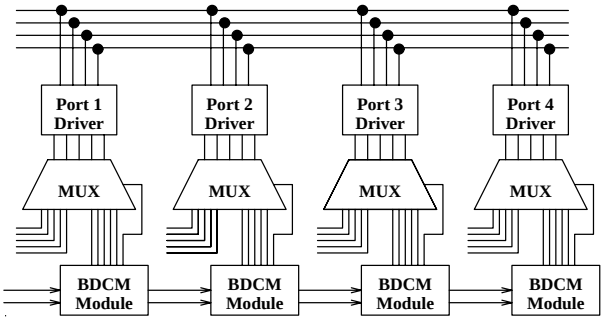

Figure 4: The BDCM architecture.

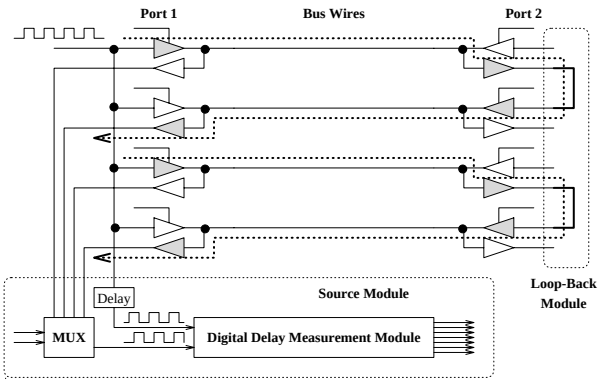

Figure 5: BDCM - the delay measurement configuration.

BDCM module serves as the gateway between internal logic blocks and bus ports. In the normal operation mode, the bus drivers are controlled by the normal operational signal. In the test mode, the bus drivers are controlled by the BDCM module.

The *delay measurement configuration* is shown in Figure 5. There is a *source module* installed on one end of the bus and a *loop-back module* installed on another end. A square wave is broadcasted to all the inputs of the source port. The test signal is received by the receiving port and looped back by the loop-back module. One of the input of the source port is selected by the multiplexer for the delay measurement. A delay element is added to counter balance the delay in the multiplexer and the loop-back control circuit at the far end. Only two drivers are enabled in each test, the rest are disabled. For this particular setup of 4 wires, two measurements are made to test half the drivers and receivers, the shaded ones. Another half can be tested by a similar configuration.

The hardware overhead for the BDCM is minimum. The overhead includes (1) a multiplexer on each port, (2) a multiplexer, an XOR gate, a delay buffer, and a counter in the source module, and (3) some switches in the loop-back module. The low hardware overhead is another distinguishing feature of the proposed methodology. With proper control and reconfiguration, the BDCM also has the diagnosis capability described below.

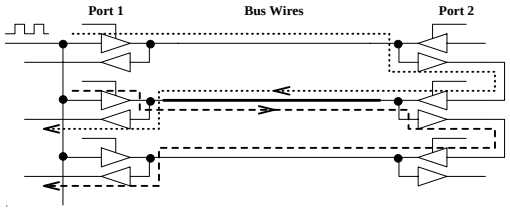


Figure 6: The wire delay fault diagnosis configuration.

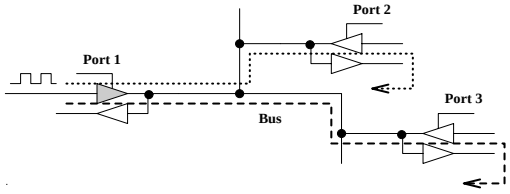


Figure 7: The driver delay fault diagnosis configuration.

## 5 Bus Delay Fault Diagnosis

With the BDCM, one is able to distinguish whether it is the driver, the receiver, or the wire that cause the delay fault. The diagnosis procedure is illustrated as follows.

- **Wire Delay Fault Diagnosis**
  The BDCM configuration and the measurement procedure shown in Figure 5 is capable for diagnosing wire delay fault. Only the wire in bold is accessed twice in two adjacent tests. If both tests fail (has longer delay), the wire is faulty. If only one test fails, either one of the drivers or receivers is faulty.

- **Driver Delay Fault Diagnosis**
  To diagnose driver delay fault, it requires the involvement of additional two ports as shown in Figure 7. After the wires are tested fault free, the test signal is looped back from different ports. The common component is the driver under consideration (shaded one). Hence, if both tests fail, the faulty element will be the driver.

- **Receiver Delay Fault Diagnosis**
  Similar to the driver fault diagnosis, additional two ports are required. As Figure 8 shows, the test signals from different sources are looped back to the receiver under consideration. Again, if both tests fail, the shaded receiver under consideration is faulty.

The above configurations show how wires, drivers, and receivers of the source module are diagnosed. The diagnosis of drivers and receivers of the loop-back modules can be achieved after the source module is tested fault-free. Since the procedure is similar to the above ones, we will not repeat here.

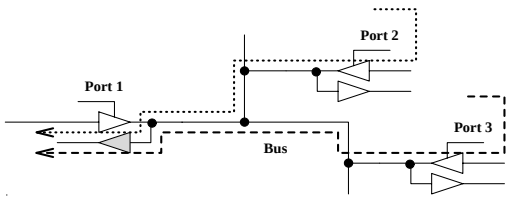


Figure 8: The receiver delay fault diagnosis configuration.

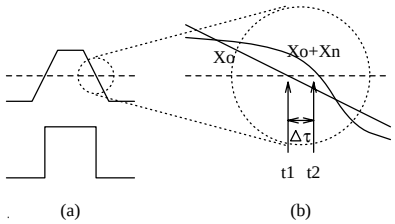


Figure 9: The crosstalk noise and jitter.

## 6 Crosstalk Measurement

### 6.1 Noise and Timing Jitter

Crosstalk is a serious problem in deep submicron technology. Unfortunately, it is also an unavoidable problem. The stray capacitance of the parallel wires will cross couple the signal from adjacent wires. Although the noise may not be large enough to alter the logic level, it creates an uncertainty in timing and poses a threat in the reliability. The uncertainty in timing is referred to as the *jitter*. Let us use the waveform in Figure 9 as an example to show the effect of crosstalk on signal timing.

Figure 9.(a) shows an input and its corresponding output waveform for the threshold of the receiver marked as the dashed line. For the enlarged transition in (b), the noise free input ($x_o$) has the transition time marked as $t_1$. For the one with a superimposed crosstalk noise $x_n$ ($x = x_o + x_n$), the transition time is $t_2$. The timing uncertainty, or jitter, is $\Delta\tau$. If the noise amplitude is $x_n$, the timing jitter can be derived as

$$\Delta\tau = \frac{x_n}{\frac{dV_s}{dt}}. \qquad (2)$$

Here, $\frac{dV_s}{dt}$ is the slop of signal transition. According to Eq. (2), the change of delay is determined by the direction and amplitude of the noise. Hence, by measuring the delay changes, we are able to obtain the amplitude of the crosstalk at the switching time. Further more, if we can control the switching time, we are able to plot the whole crosstalk profile by multiple delay measurement.

### 6.2 BDCM Crosstalk Measurement Configuration

Based on the above derivation, the propose crosstalk measurement configuration is shown in Figure 10. Basically, it shares the similar hardware with the delay measurement configuration. The additional modules are listed as follows. First, the *timing generation module* (TGM) is a buffer chain that generates the test signals with different timing $t_i$. The number of stages must be large enough to cover the duration of the crosstalk effects. The *timing select module* (TSM) is a multiplexer that applies the wire under consideration a test signal with proper timing. The *polarity select module* (PSM) is a exclusive-or gate that control the polarity of the test signal. If P is 1, the adjacent

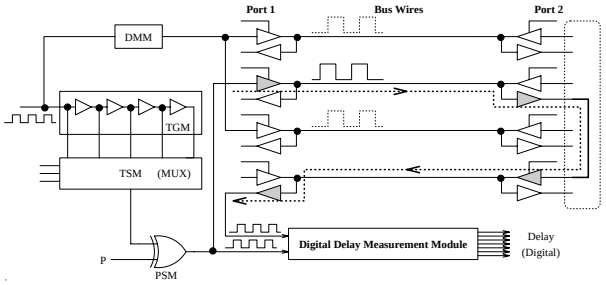

Figure 10: The crosstalk measurement architecture.

lines have different polarity as the line under consideration and vise versa for P of 0. The *delay match module* is a buffer to match the delay incurred in the TSM and PSM.

The crosstalk measurement proceeds as follows.

**Step 1 - Calibration** :
The timing of all the stages in the TGM are calibrated by the delay measurement module presented earlier.

**Step 2 - Intrinsic Delay Measurement** :
The intrinsic delay $\tau_o$ is measured when adjacent wires are kept silent without signal switching. The signal path is marked with bold dotted line.

**Step 3 - In-phase Crosstalk Measurement** :
P is set to 0 and the delays ($\tau_{0i}$) are measured for the signal with a delay of $t_i$.

**Step 4 - Out-phase Crosstalk Measurement** :
P is set to 1 and the delays ($\tau_{1i}$) are measured for the signal with a delay of $t_i$.

In Step 3 and 4, the relative delay, $\Delta\tau_{pi} = \tau_{pi} - \tau_o$ represents the effect of crosstalk at $t_i$. After repeating Step 3 and 4 for different timing $t_i$, the delay profiles with respect to the crosstalk can be obtained.

## 7 Simulation Results

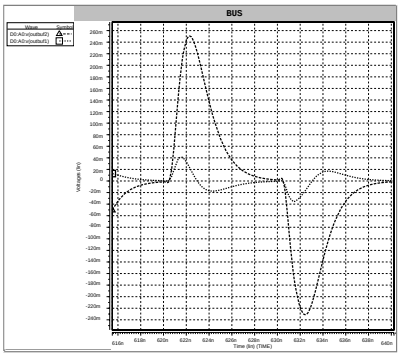

Figure 11: The crosstalk waveforms.

The SPICE simulation results on the proposed delay and crosstalk measurement are presented in this section. The parameters are obtained either from our measurement results or those extracted from [4, 5]. The key parameters include a unit-length resistance of $40\Omega/cm$, a unit-length to-ground capacitance of $1pF/cm$, and a unit-length adjacent-wire coupling capacitance of $1pF/cm$. The bus is $1cm$ long which is decomposed into 10 segments as the model shown in Figure 1. The resistance and capacitance are evenly distributed into these segments. The drivers and the receivers are designed for a 200MHz operation with 20% safety margin.

Figure 11 shows the crosstalks coupled from the immediate neighbor wire (dashed line) and from the next neighbor wire (dotted line). Here, the victim wire is pulled down. The peak crosstalk voltage is 0.25V from the immediate neighbor.

As the stated earlier, the crosstalk will affect the delay of the test signal. Figure 12 shows the test signals on the wire with and without the crosstalk. The rectangle one is the input test signal at the driver. The rests, from left to right, are the signals on the wire when the adjacent wires are (1) switching in the same direction, (2) not switching , and (3) switching in the opposite direction. Figure 13 shows the received signals at the receiver output in the same order. The delay varies from $1.9ns$ to $3.9ns$. As one can see, with a crosstalk as small as $\pm 0.25V$, the delays vary from $1.9ns$ to $3.9ns$. This reassures that the crosstalk is a major reliability issue and the crosstalk measurement is indispensable. This also hints that the use of delay for crosstalk measurement is feasible.

Figure 14 shows the crosstalk delay profiles obtained by the proposed method. The X axis is the switching timing of the test signal ($t_i$) and the Y axis is the timing jitter $\Delta\tau_{pi}$. Two curves are presented, one for the low-to-high transition (solid line) and another for the high-to-low transition (dashed line).

The negative humps ($-2ns$ to $8ns$) are the results when adjacent wires are switching in the same direction as the wire under consideration. Since, the crosstalk helps the wire make the switching, the delay is reduced. The maximal reduction of $\Delta\tau_{0max}$ is about $1ns$ when $t_i$ is $1ns$. The effect of crosstalk starts when the signal is $-2ns$ ahead of the adjacent wire switching. This is quite natural for an intrinsic delay of $2.7ns$. The positive humps ($8ns$ to $18ns$) are the results of the opposite direction switching of the adjacent wires. They are similar to the previous ones in shape except for a larger delay changes of $1.5ns$ at the falling edge and $1.25ns$ at the rising edge.

Comparing Figure 11 and 14, one can see that their shapes are similar and their polarities are different. The test demonstrates that the relationship between delay and crosstalk being claimed is valid. It also indicates that one is able to use the crosstalk delay profile to derive the crosstalk noise waveform. The differences between the rising edge and fall edge profiles are due to the differences between the high/low driving capabilities of the driver and the logic threshold values of the receiver. With the crosstalk delay profiles, design or process engineers are able to know how to redesign the circuit or improve the process to optimize the performance.

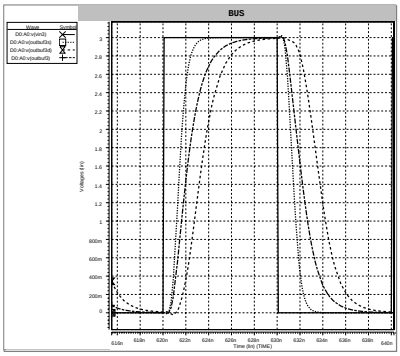


Figure 12: The test signal waveforms - on the bus.

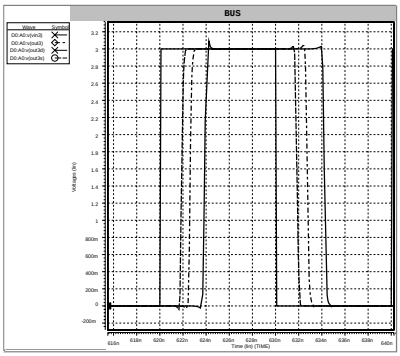


Figure 13: The test signal waveforms - at receiver output.

## 8 Conclusions

In this paper, a methodology has been proposed for the delay and the crosstalk measurement of deep submicron on-chip buses. First, a digital delay measurement technique has been derived. It is based on the detail statistical analysis on the random sampling of the periodical timing difference signal. Second, based on the proposed methodology the BDCM architecture has been proposed and designed. The hardware overhead is extremely low with a multiplexer, an XOR gate, a counter, a delay buffer, and some switches only. Third, three diagnosis configuration have been proposed based on the BCDM architecture. With which, the delay faults in driver, receiver, or wire can be identified. Forth, the BDCM is used for the crosstalk measurement with little modification. The relationship between delay and crosstalk has been studied in detail to derive the metrology of the crosstalk profile.

The proposed methodology has been verified by the SPICE simulation. A wire resistance of $40\Omega/cm$, a wire capacitance of $1pF/cm$, and a coupling capacitance of $1pF/cm$ have been used for the bus model [4]. The test results show that a subtle crosstalk noise of $0.25V$ is able to alter the delay from $1.9ns$ to $3.9ns$. The matching of the crosstalk delay profile and the crosstalk noise profile demonstrates the feasibility of the BDCM. One is able to use the crosstalk delay profile as the crosstalk noise profile for testing and diagnosis purposes.

The BDCM has the following distinguished features. First, the all digital design makes it the technology independent and easily portable. Second, the circuit structure is very simple. Third, it does not interfere with the operation of the buses and need not to modify the design of the bus wire, driver and receiver design. The methodology is not limited to on-chip buses only. The same technique can be applied to on-board or system level interconnect testing and diagnosis as well.

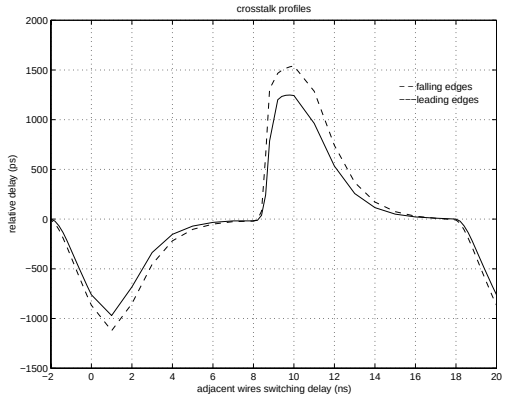


Figure 14: The measured crosstalk delay profile.

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