Alternative Test Methods Using IEEE 1149.4

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Abstract

IEEE 1149.4 infrastructure has been aimed primarily for printed circuit board (PCB) interconnect test, parametric test of discrete components and functional test of IC cores. Methods to perform these tests have been published and experimental results using evaluation samples of IEEE 1149.4 ICs have been reported. So far, most attention has been paid to test and measurement techniques for the first two issues. Proposed methods typically employ IEEE 1149.4 infrastructure in the function of a built-in test probe that enables external test and measurement equipment to access the internal PCB points via the analog test bus

This paper describes an alternative approach based on functional transformation of the tested board by means of the existing IEEE 1149.4 resources. In this way, efficient go no-go functional test can be performed. Case studies are given to illustrate the proposed approach.

1. Introduction

The aim of the IEEE 1149.4 Standard for a Mixed-Signal Test Bus, [1], recently approved by the IEEE-SA Standards Board is to provide standardized approaches to interconnect test, parametric test and internal test. For the first objective, the aim is to provide facilities that allow to detect opens in the interconnections between integrated circuits, and to detect and localize bridging faults. The second objective refers to the problem of measuring the values of discrete components such as pull-up resistors, filter capacitors, etc., that are often interposed between integrated circuits on a board. The third objective relates to the ability to perform internal test of a component. An internal test of a complex component mounted on a board may result in a rather costly testing procedure, hence this option of the proposed standard is not mandatory. IEEE 1149.4 can be regarded as an extension of IEEE 1149.1 Std by providing Analog Boundary Modules (ABMs) in each functional pin of analog and mixed-signal ICs.

In the course of preparation of IEEE 1149.4, papers covering general issues of the new standard have been published, [2]-[4]. Some experimental test chips have been implemented [5]-[7] and feasibility studies have been performed [8]-[13]. Methods primarily concerned with parametric test of discrete components on a PCB have been proposed [15]-[20]. They employ IEEE 1149.4 infrastructure in a function of a built-in test probe that enables external test and measurement equipment to access internal PCB points via the analog test (AT) bus.

This paper describes an alternative approach based on functional transformation of the tested board by means of the existing IEEE 1149.4 resources. In this way, efficient go no-go functional test can be performed. The proposed approach is illustrated by three case studies from different application domains.

2. Functional transformations by means of IEEE 1149.4 infrastructure

Beside PCB interconnect test and parametric test of discrete components IEEE 1149.4 infrastructure provides means for implementation of functional tests of separate IC cores as well as arbitrary parts of PCB. In the latter case, selected functional parts can be organized in a self-test structure performing efficient go no-go functional test. As shown in the first case study, external circuitry can be applied via AT bus to form a simple and effective test environment. An external circuit (or just a passive component) applied via AT bus can also serve for changing the operating conditions of the unit-under-test. This can be helpful in different cases, like for example, simulating operating conditions of sensor circuits as shown in the second case study. Finally, the third example describes a situation where IEEE 1149.4 infrastructure is employed to enhance controllability and observability of multistage circuits.

2.1. Performing functional test by applying external circuitry via AT bus

Even if the new IEEE 1149.4 Standard gets full support from manufacturers it is realistic to expect that most mixed-signal PCBs in practice will contain clusters with nodes that are not directly accessible from the boundary ABMs. Like in the case of digital boundary-scan testing, ad-hoc test solutions will take advantage of IEEE 1149.4 resources at the cluster boundary.

Consider, for example, a PCB with a cluster consisting of the active RC filter depicted in Figure 1. Let us assume that only Vin and Vout pins are directly connected to the boundary ABMs. One of the possible ways of testing this circuit can be the oscillation test method [21], [22].

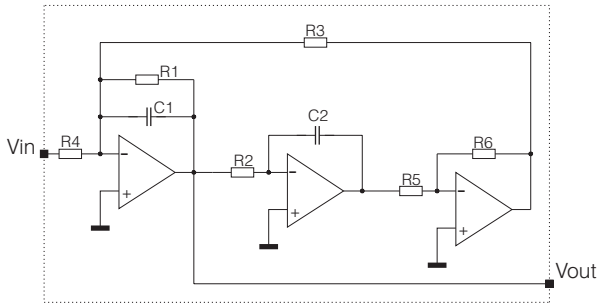

Figure 1. PCB cluster - active RC filter

If we connect the filter to the external circuit shown in Figure 2, the circuit will oscillate at the frequency of the pole which inherently reflects the characteristics of the filter stage. The external circuit provides the required phase shift and gain to put cluster into oscillation. Comparing the measured frequency to a reference value obtained from a known-good unit one can perform a functional test of the cluster.

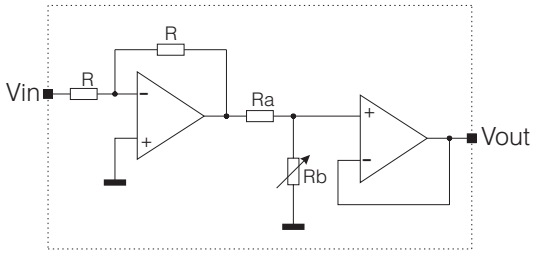

Figure 2. External circuit

The salient feature of this example is the fact that IEEE 1149.4 AT bus is employed to connect the external circuit to the terminals of the filter stage as shown in Figure 3.

For experimental purposes, the filter stage and the external circuit were implemented on separate PCBs. The filter stage had a pole at 1323 Hz. When directly connected to the external circuit, R_b was actively adjusted to achieve the minimum gain for the oscillation. Next, the two circuits were connected via AT bus of IEEE (IMP) Demo Chips [5] as shown in Figure 3. In this way, the situation of a cluster surrounded by ABMs was simulated.

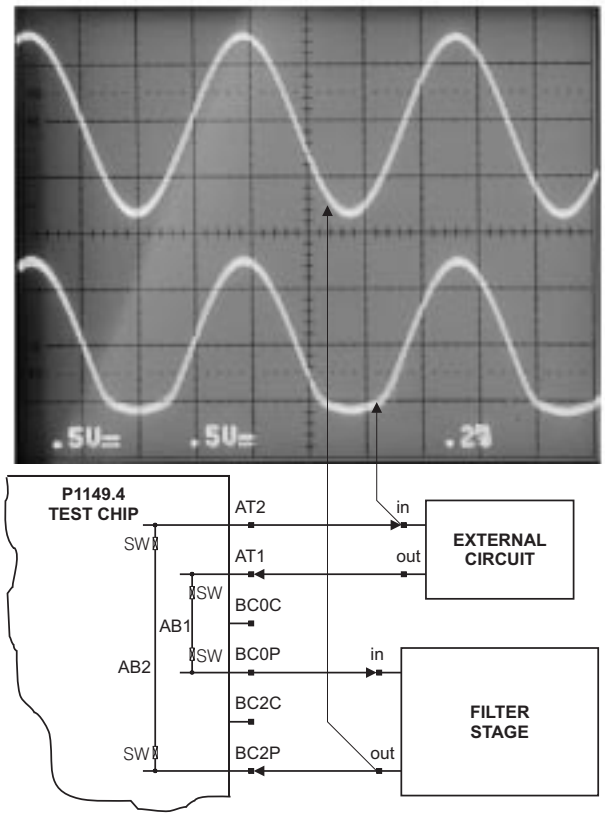

Figure 3. Experiment conducted via AT bus

As expected, the gain had to be adjusted when AT bus was employed (Table 1). However, the resulting oscillating frequency (measured by a counter) was the same in both cases which confirms the applicability of the approach.

Table 1. Measurement results

	R_b [kΩ]	f_{OSC} [Hz]
Direct connection	241	1323
Via AT bus	297	1323

2.2. Changing operating conditions in system functional test

System functional test should be normally performed in the conditions closely resembling the application in practice. Testing in the real target environment is often impractical hence other possibilities are explored. A simple low-cost solution for changing the operating

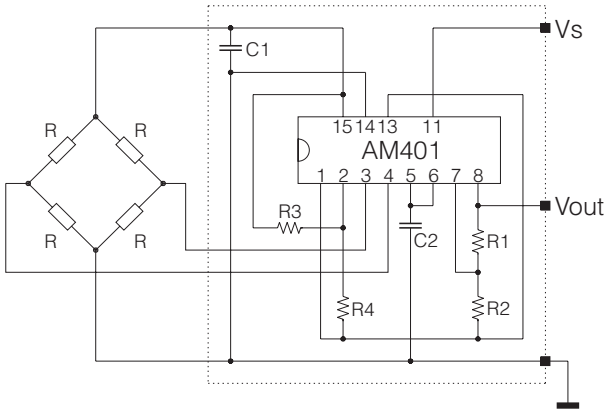

Figure 4. Pressure sensor transmitter circuit

conditions of a system-under-test is to vary the values of electrical parameters (signals) conditioned by the external environment and in this way simulate the situation in real world. This may not always be easy to accomplish hence the system should be designed-for-testability in this respect. The IEEE 1149.4 infrastructure can be employed for this purpose as demonstrated in the following example.

Suppose that a pressure sensor consisting of a piezo-resistive sensor chip die connected to a monolithic voltage transmitter shown in Figure 4 is a part of a mixed-signal PCB. Let us assume that the signal from the output of the pressure sensor determines the operating conditions of the system-under-test. For a consistent functional test proper pressure must be applied which may not always be convenient. The same effect can be achieved by unbalancing the bridge with an additional resistor parallel to R. This may pose a problem due to the packaged pressure sensor. However, if the voltage transmitter IC was conformant with IEEE 1149.4, the resistor could easily be applied via AT bus (for example, between pins 4 and 15). In the latter case, one must take into account the impedance of the AT bus. For the pressure sensors with bridge resistors in the range of 400 Ω - 4kΩ and additional resistor of higher values, the impedance of AT bus does not seem to be restrictive. Yet, as stated in [4], the impedance of AT bus of a device supporting IEEE 1149.4 Standard must be documented so that the test generation tools can take these internal values into account when computing expected results.

2.3. Enhancing controllability and observability of multistage circuits

Multistage circuits (either digital or analog) are typical candidates for the introduction of boundary-scan path to enhance their controllability and observability. Implementation of tests of individual stages is of course a designer's freedom - it can be done in a number of ways. IEEE 1149.4 Standard provides means to access individual parts separately, it also alows reconfiguration of arbitrary parts into a self-testing structure. One possible example is described in the following.

Consider a 6^{th} order bandpass SC filter that can be realized as a cascade of three second-order (biquad) bandpass stages, featuring adequate pole frequencies (f_0) and quality factors (Q). In order for the stages to be tested separately, access to the stage input from a primary input and to a primary output form the stage output has to be provided [23]. For this purpose, IEEE 1149.4 analog test bus infrastructure is built-in, as illustrated in Figure 5.

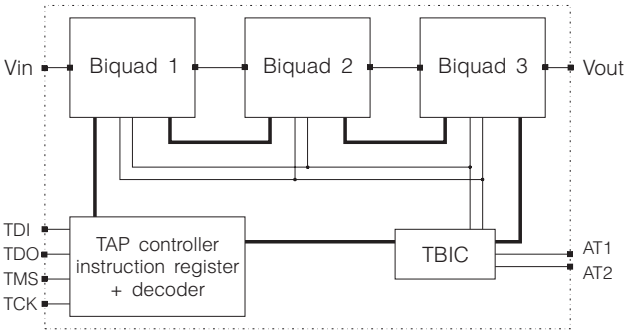

Figure 5. SC filter with IEEE 1149.4 infrastructure

The resulting structure enables the conventional way of testing separate stages by applying external stimulus and measuring the output via AT bus. Besides, available test infrastructure also provides means to employ the oscillaton test method with minimum hardware overhead: the necessary condition to put a filter stage into oscillation is to switch off capacitor C_C, Figure 6 (more details on this issue are given in [24]).

The oscillation test structure of a filter stage can be implemented by means of two ABMs built into each stage (except for the final stage, which requires an additional ABM), as illustrated in Figure 6, allowing for separate testing of single stages. Here *C* denotes the ABM terminal which is usually connected to the analog core, while *P*

denotes the terminal, usually connected to the pin of the component.

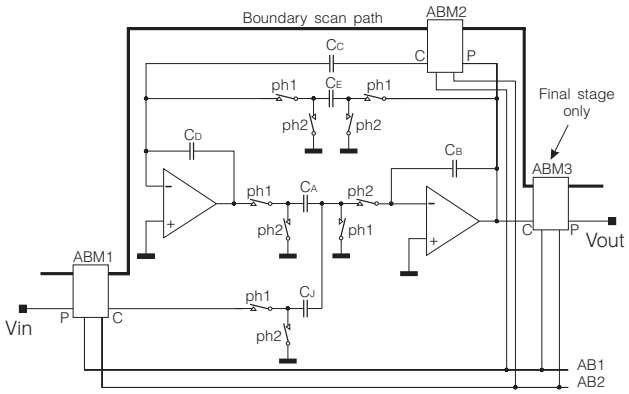

Figure 6. SC filter stage with built-in ABMs

The stage under test is isolated from the previous filter stage or from external circuitry by switching off SD in ABM1. The stage output can be isolated from the following filter stage or from external circuitry by switching off SD of the next stage ABM1 or the one in ABM3 respectively. The SD switch in ABM2 is used to switch off capacitor C_C, while the stage output can be connected to AT1 or AT2 via switches SB1 or SB2 of ABM2, thus providing the facility to actually measure the frequency of the oscillating stage under test (SD, SB1 and SB2 refer to the ABM switch structure described in [1].)

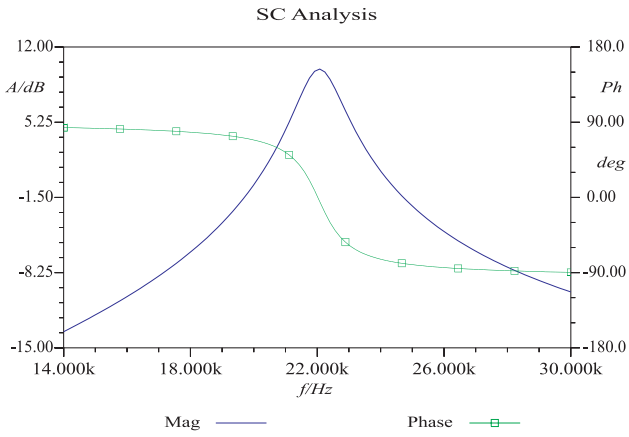

Figure 7. Frequency response simulation of SC filter stage under normal operation

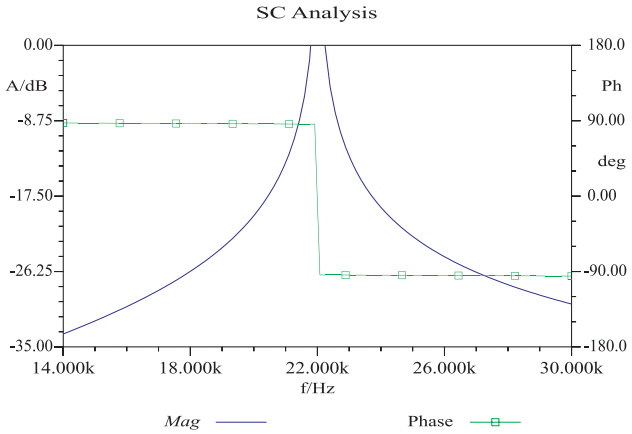

Figure 8. Frequency response simulation of SC filter stage under test mode

Figure 7 gives the frequency response characteristics of the SC biquad in its normal operation and Figure 8 in the test mode, respectively. As the simulation results show, the oscillation frequency matches the designed pole frequency of the filter stage. Obtained results are just the first approximation - the actual implementation of the designed SC filter will require accurate modeling of parasitic capacitances and resistances introduced by the ABMs. Although this may affect to some extent the actual filter parameters, the basic test approach remains essentially the same.

Solution presented in the above example can be regarded as the first step toward the implementation of a built-in self-test. The second part would comprise a circuitry for measuring the difference of the oscillating frequency from the predetermined reference value which can be implemented by a simple digital counter and some additional logic. Realization of such structure is purely digital and is not subject of this paper.

3. Conclusions

IEEE 1149.4 infrastructure offers a variety of effective solutions to the problem of functional testing of analog and mixed-signal systems. The proposed approach based on functional transformation of individual parts of the system-under-test can be applied in different situations in practice as demonstrated by the illustrative examples in the paper. Although the advantages of the described approach differ from one case to another, they have in common a simplified generation of stimulus and consequently a simplified test procedure.

Performed experiments were inevitably limited to the cases that could be handled by the available test ICs. Likewise the assumptions regarding the analog parametric

limits of the IEEE 1149.4 infrastructure which implicitly reflect in the proposed solutions could only be verified on the existing test IC samples. For these reasons the selected examples were performed within "safe" low frequency range and in the operating conditions where the impedance of the analog test bus did not present a critical factor.

Real applications will become feasible with the introduction of the devices supporting the IEEE 1149.4 standard from the major manufacturers of mixed-signal and analog ICs. Analog parametric limits imposed by the commercially available ICs are likely to be less restrictive due to the full integration of IEEE 1149.4 infrastructure within the circuit. Therefore designers will have more freedom in applying reconfiguration strategies in practice.

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