A New Approach for Computation of Timing Jitter in Phase Locked Loops

M M. Gourary[(1)], S. G. Rusakov[(1)], S. L. Ulyanov[(1)], M.M. Zharov[(1)], K. K. Gullapalli[(2)], and B. J. Mulvaney[(2)]

(1) IPPM, Russian Academy of Sciences, Moscow

(2) Motorola Inc., Austin, Texas

Abstract

A new method for computation of timing jitter in a PLL is proposed. The computational method is based on the representation of the circuit as a linear time-varying system with modulated stationary noise models, spectral decomposition of stochastic process and decomposition of noise into orthogonal components i. e. phase and amplitude noise. The method is illustrated by examples of jitter computation in PLLs.

1. Introduction

Phase Locked Loop (PLL) circuits are widely used components in modern communication electronics [1,2]. The main problems of PLL design are related to the simulation of nonlinearities and noise. The development of numerical procedures for noise simulation in a PLL is an open problem due to the complexity and peculiarities of a PLL. Timing jitter is the main noise characteristic of a PLL [3], and affects the timing accuracy and the signal to noise ratio in circuits based on a PLL. Clearly, estimating jitter is important for the design of PLLs, frequency synthesizers, clock recovery circuits, etc.

The complexity of PLL circuits led several authors to noise simulation methodologies based primarily on behavioral level simulation (see for instance [4, 5, 6, 7, 8]). In particular the methodology in [4] uses a transient noise analysis of each of the PLL blocks and converts the obtained noise responses to jitter.

In contrast to these publications, this paper presents a method for computing the noise response of the full PLL at the circuit (transistor) level, providing noise analysis of a PLL in a conventional Spice-like simulator.

Numerical procedures for timing jitter computation at the transistor level have been investigated in detail for autonomous circuits [9]. However, the PLL is the driven circuit. The present approach is based on a numerical technique [10] which provides noise analysis of nonlinear circuits in the time domain. In contrast to the approach presented in [11], no time-consuming convolution-like procedures involving a transfer function are used.

It can be noted also that many of the previous approaches to PLL noise simulation have some limitations in terms of flicker noise. The present approach in comparison, for instance with [12], allows us to take into account the flicker noise sources without additional computational efforts.

Section 2 presents the formulation of timing jitter in the case of driven circuits. The basic numerical procedure is presented in Section 3. Some experimental results of timing jitter computations in a PLL are presented in section 4.

2. The concept of timing jitter

The problem of noise simulation in PLL is a special case of jitter analysis of nonlinear driven systems in time domain.

The following expression is used to estimate timing jitter value in a cell of ring oscillator [2]:

$$\overline{dt}^2 = \overline{dv}^2 / (SlewRate)^2 \qquad \text{(eq. 1)}$$

Here *dv* is the perturbation of the transient waveform due to noise computed at the transition and *SlewRate* is determined by the slope of the transient waveform.

In oscillators this timing jitter determines the starting point of the next cycle and therefore creates a permanent phase shift in the output signal [3]. With each cycle of oscillation, the jitter variance continues to grow. Timing jitter in a PLL depends on the interaction of noise in the oscillator with the dynamics of the phase-locked loop because the phase difference is compensated by the feedback of the loop. Such a distinction between oscillator and PLL circuits is taken into consideration below.

To determine timing jitter in a PLL we extend the methodology of jitter estimation in free-running oscillators [4] to the case of closed-loop oscillators i.e. PLL.

Timing jitter *J* can be considered as a discrete time

stochastic process with the following probabilistic characterization [4]:

$$E[J(k)^2] = \frac{E[y(\tau_k)^2]}{S_k^2} \qquad \text{(eq. 2)}$$

where y is the noise response and S_k is the maximal value of large signal time derivative at the output node estimated over time interval T, and τ_k is the corresponding time point.

According to this formula, to compute the variance of the timing jitter the following steps are performed:

1) determine large signal solution and derivatives.

2) apply transient noise analysis to compute noise response and its variance. For PLL circuits this analysis is performed while splitting the total noise into normal and tangential parts.

3) determine maximal derivatives in the interval T.

4) sample the noise variance and compute the timing jitter variance using expression (2).

The basic numerical procedure to compute noise response in transient noise analysis (step 2) is presented next.

3. Computational method

The computational scheme for phase noise evaluation is founded on the combination of the approach to transient noise (TRNO) analysis [10] and noise decomposition into orthogonal components (amplitude and phase noise) [13].

The nonlinear circuit can be described by the following equation:

$$\dot{q}(x(t)) + i(x(t)) + b(t) + Au(t) = 0 \qquad \text{(eq. 3)}$$

where $q(x)$, $i(x)$ are vectors of node charges or fluxes, $b(t)$, $u(t)$ are vectors of large signals and noise sources respectively (the N *by* K matrix A reflects the connections of noise sources). The vector $x(t)$ includes node voltages and some branch currents.

Assuming the contribution of the noise sources is small, the equation can be linearized about the large-signal noise-free solution $x_L(t)$ giving the following equation with respect to the vector of noise response $y(t)$:

$$C(t)\dot{y}(t) + G(t)y(t) + Au(t) = 0 \qquad \text{(eq. 4)}$$

$$\text{where } C(t) = \frac{\partial}{\partial x} q(x_L(t)) \qquad \text{(eq. 5)}$$

$$G(t) = \frac{\partial}{\partial x} i(x_L(t)) + \frac{d}{dt} C(t) \qquad \text{(eq. 6)}$$

Equation (4) is a linear differential system with time-varying coefficients and therefore the overall noise response can be computed as the superposition of noise responses to every noise source:

$$y(t) = \sum_{k=1}^{K} y^{(k)}(t) \qquad \text{(eq. 7)}$$

To obtain equations for noise response, the spectral decomposition for noise sources is used:

$$u^{(k)}(t) = \sum_{l=1}^{L} \xi_l^{(k)} s^{(k)}(\omega_l, t) e^{j\omega_l t} \qquad \text{(eq. 8)}$$

Here $s^{(k)}(\omega_l, t)$ is square root of modulated spectral density, $\xi_l^{(k)}$ are uncorrelated random values with variance $\Delta\omega_l$, where $\Delta\omega_l = \omega_l - \omega_{l-1}$ is the frequency interval.

Inserting (8) into (4) and using the substitution

$$y^{(k)}(\omega_l, t) = z^{(k)}(\omega_l, t) e^{j\omega_l t} \qquad \text{(eq. 9)}$$

the following basic equations for the noise response are obtained [10] :

$$C(t)\dot{z}^{(k)}(\omega_l, t) + (G(t) + j\omega_l C(t)) z^{(k)}(\omega_l, t) + as^{(k)}(\omega_l, t) = 0 \qquad \text{(eq. 10)}$$

$l=1,2,...,L$ and $k=1,2,...,K$ that should be integrated in time interval of interest.

Experimental analysis showed that the direct application of these equations to PLL noise simulation is difficult due to the instability of numerical integration (10) by standard Spice integration techniques. To solve this problem we decompose the total noise response into two orthogonal components. The performed analysis confirmed that this separation allowed us to avoid the integration instability.

Let the noise response $y(t)$ be split into normal and tangential parts [13]:

$$y(t) = y_{\perp}(t) + y_t(t) \qquad \text{(eq. 11)}$$

where

$$y_t(t) = x(t + \theta(t)) - x(t) \qquad \text{(eq. 12)}$$

Here $\theta(t)$ determines random phase fluctuation. This function describes the phase process. It determines a stochastic time shift and can be used for characterization of time uncertainty of analyzed circuit.

After linearization of (12) with respect to $\theta(t)$ we can obtain the following expressions:

$$y_t(t) = \dot{x} \cdot \theta \qquad \text{(eq. 13)}$$

$$\dot{y}_t(t) = \ddot{x} \cdot \theta + \dot{x} \cdot \dot{\theta} \qquad \text{(eq. 14)}$$

Inserting (11) into (4) we can obtain

$$\begin{gathered} C(t)\dot{y}_{\perp}(t) + G(t)y_{\perp}(t) + \\ C(t)\dot{y}_t(t) + G(t)y_t(t) + Au(t) = 0 \end{gathered} \qquad \text{(eq. 15)}$$

Taking into account expressions (13), (14) the equation (15) yields

$$\begin{gathered} C(t)\dot{y}_{\perp}(t) + G(t)y_{\perp}(t) + (C(t)\ddot{x} + G(t)\dot{x})\theta + \\ C(t)\dot{x}\dot{\theta} + Au(t) = 0 \end{gathered} \qquad \text{(eq. 16)}$$

To simplify (16) we can derive, by differentiating (3) with respect to time, the following useful equation:

$$C(t)\ddot{x}(t) + G(t)\dot{x}(t) + \dot{b}(t) = 0 \qquad \text{(eq. 17)}$$

This expression is obtained assuming noise sources to be zero in (3). Taking into account expression (17) we can finally obtain:

$$\begin{gathered} C(t)\dot{y}_{\perp}(t) + G(t)y_{\perp}(t) + \\ (C(t)\dot{x})\dot{\theta} + (-\dot{b})\theta + Au(t) = 0 \end{gathered} \qquad \text{(eq. 18)}$$

The system (18) has an additional variable θ. To complete (18) we add an equation derived from the condition of orthogonality:

$$\dot{x}^T \cdot y_{\perp} = 0 \qquad \text{(eq. 19)}$$

The expressions (18) and (19) are the basic equations for phase noise or jitter simulation. It is important to note that the solution $\theta(t)$ can be directly applied to estimate timing jitter:

$$E[J(k)^2] = E[\theta(\tau_k)^2] \qquad \text{(eq. 20)}$$

Experiments show that the expression (20) is consistent with the general concept of timing jitter. In particular, (20) is equivalent to the expression (2) in the case of dominant contribution of phase noise:

$$|y_{\perp}(\tau_k)| \ll |y_t(\tau_k)| \qquad \text{(eq. 21)}$$

For this reason time points τ_k chosen from the condition of minimal ratio $|y_{\perp}|/|y_t|$ are equivalent to maximal derivative time points. Therefore in practice the expression (20) gives the same results as expression (2).

To solve the system (18), (19) we use the same approach that was used to solve (4). Namely, the noise sources are presented by modulated spectral decomposition and considered independently. Then we can write

$$y_{\perp}(t) = \sum_{k=1}^{K} \sum_{l=1}^{L} \tilde{\xi}_l^{(k)} \cdot z_{\perp}{}^{(k)}(\omega_l, t) e^{j\omega_l t} \qquad \text{(eq. 22)}$$

$$\theta(t) = \sum_{k=1}^{K} \sum_{l=1}^{L} \tilde{\xi}_l^{(k)} \cdot \varphi^{(k)}(\omega_l, t) e^{j\omega_l t} \qquad \text{(eq. 23)}$$

where $\tilde{\xi}_l^{(k)}$ are coefficients of decomposition (8).

The values $z_{\perp}, \varphi$ are obtained by solving of equations:

$$\begin{gathered} C(t)\dot{z}_{\perp}{}^{(k)}(\omega_l, t) + \\ (G(t) + j\omega_l C(t))z_{\perp}{}^{(k)}(\omega_l, t) + \\ (C(t)\dot{x}(t))\varphi^{(k)}(\omega_l, t) + \\ (-\dot{b}(t) + j\omega_l C(t)\dot{x}(t))\varphi^{(k)}(\omega_l, t) + \\ as^{(k)}(\omega_l, t) = 0 \end{gathered} \qquad \text{(eq. 24)}$$

$$\dot{x}^T(t) z_{\perp}{}^{(k)}(\omega_l, t) = 0 \qquad \text{(eq. 25)}$$

These equations are solved using implicit integration techniques. It is important that solutions of these equations are smoother than the solutions of (10). This makes it practical to estimate the variance of timing jitter in a PLL.

The variance of the total noise at a certain node of the circuit can be computed using the following expression [10]:

$$E[y(t)^2] = \sum_{l=1}^{L}\sum_{k=1}^{K}\left|z_{\perp}^{(k)}(\omega_l, t) + \varphi^{(k)}(\omega_l, t)\cdot\dot{x}(t)\right|^2\cdot\Delta\omega_l \qquad \text{(eq. 26)}$$

Similarly, the time dependence of jitter variance is computed by the following expression:

$$E[\theta(t)^2] = \sum_{l=1}^{L}\sum_{k=1}^{K}\left|\varphi^{(k)}(\omega_l, t)\right|^2\cdot\Delta\omega_l \qquad \text{(eq. 27)}$$

where $\Delta\omega_l = \omega_l - \omega_{l-1}$ the frequency interval.

The presented computational scheme can be easily implemented in a conventional Spice-like circuit simulator.

4. Experimental results

To provide a special-purpose mode for nonstationary noise simulation, the described approach has been implemented in a Spice-like simulator.

This section presents some results of computation of jitter in a PLL circuit. The 560B PLL circuit is taken from [1], and it contains a VCO, loop filter, and phase detector, all implemented with 32 bipolar transistors, 9 diodes and 31 linear components.

The computation of timing jitter includes determining steady-state solution for large signal, integration of noise equations (24), (25) with simultaneous calculation of jitter using expression (20). The computed jitter is shown in the figures for several periods of time.

Fig. 1 illustrates the effect of temperature on the jitter in this PLL, jitter characteristics computed at the temperature of 27 degrees and 50 degrees of centigrade without flicker noise are given. The computed temperature dependence of jitter is shown in the fig. 2.

The effect of flicker noise on timing jitter in PLL circuit is demonstrated by fig. 3 (simulation without flicker noise and with flicker coefficient 10^{-11}). It is important to note that these results are obtained without additional computational efforts.

Fig. 4 illustrates the capability to investigate the dependence of timing jitter on parameters of PLL. In particular fig. 4 demonstrates the reduction of the jitter with increase of the loop bandwidth. Jitter is approximately inversely proportional to the bandwidth of the PLL [3].

5. Conclusion

The suggested approach to nonstationary noise simulation and the corresponding computational scheme allows us to perform jitter simulation in a PLL using a standard Spice like simulator. In comparison with known results the jitter is evaluated at the transistor level using modulated stationary noise models.

The present method allows us to perform PLL noise simulation taking into account flicker noise without additional computational efforts.

6. References

[1] P. Gray, R. Meyer, *Analysis and Design of Analog Integrated Circuits*, John Wiley & Sons, 1984.

[2] T.C. Weigandt, B.Kim, P.R. Gray "Analysis of Timing Jitter in CMOS Ring Oscillators", in Proc. ISCAS, vol. 4, pp. 27-30, 1994.

[3] B.Kim, T.C. Weigandt, P.R. Gray, “PLL/DLL System Noise Analysis for Low Jitter Clock Synthesizer Design”, ISCAS, June 1994.

[4] A. Demir, A. Sangiovanni-Vincentelly, *Analysis and Simulation of Noise in Nonlinear Electronic Circuits and Systems*, Kluwer Academic Publishers, 1997.

[5] A. Demir, E.Liu, A. Sangiovanni-Vincentelly, and L. Vassiliou, “Behavioral Simulation Techniques for Phase/Delay-locked Systems”, in Proc. of the IEEE Custom Integrated Circuits Conf., May 1994, pp. 453-456.

[6] K. Kundert, “Modeling and Simulation of Jitter in PLL”, in Advances in Analog Circuit Design, 1997.

[7] B.S.Smedt, G. Gielen, “Nonlinear Behavioral Modeling and Phase Noise Evaluation in PLL”, in Proc. of the IEEE Custom Integrated Circuits Conf., 1998, pp. 53-56.

[8] M. Takahashi, K. Ogawa, K. Kundert, “VCO Jitter Simulation and Its Comparison With Measurement”, ASP-DAC'99, 1999.

[9] A. Demir, A. Mehrotra, J. Roychowdhury, “Phase Noise in Oscillators: A Unified Theory and Numerical Methods for Characterisation”, Proc. 35-th DAC, 1998.

[10] M. M. Gourary, S. G. Rusakov, S. L. Ulyanov, M. M. Zharov, and B. J. Mulvaney, ”A New Method for Transient Noise Analysis”, in Proc. ASP-DAC, 1999, pp.165-168.

[11] M. Okumura, H. Tanimoto, T. Itakura, T. Sugawara, "Numerical Noise Analysis for Nonlinear Circuits with a Periodic Large Signal Excitation Including Cyclostationary Noise Sources", IEEE Trans. on Circuits and Systems - I, vol. 40, N 9, 1993, pp. 581-590.

[12] A. Demir, E. Liu, A. Sangiovanni-Vincentelli, "Time-domain non Monte-Carlo noise simulation for nonlinear dynamic circuits with arbitrary excitations," IEEE Trans. on Computer-Aided Design, vol. 15, 1996, pp. 493-505.

[13] F.X. Kaertner, "Determination of the Correlation Spectrum of Oscillators with Low Noise ", IEEE Trans. on Microwave Theory and Techniques, vol. 37, N 1, 1989, pp.90-101

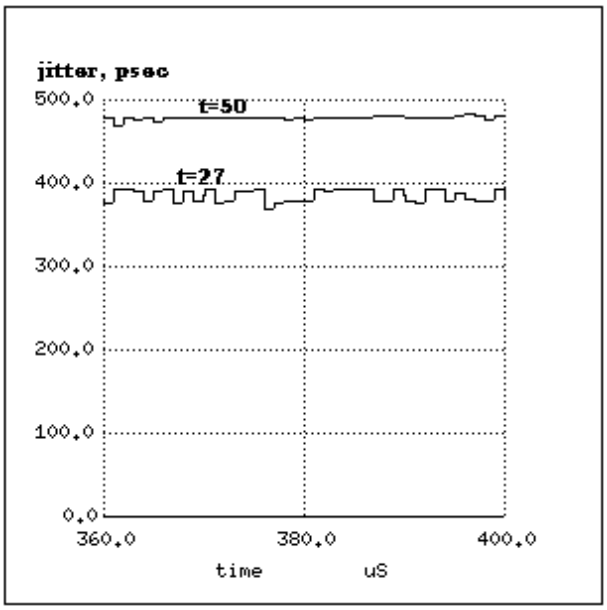

Figure 1. rms jitter for 27 and 50 degrees

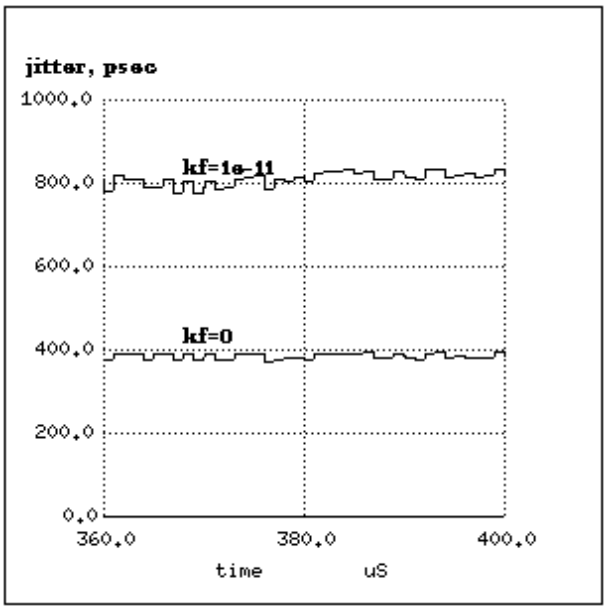

Figure 3. rms jitter without and with flicker noise (coefficient 10^{-11})

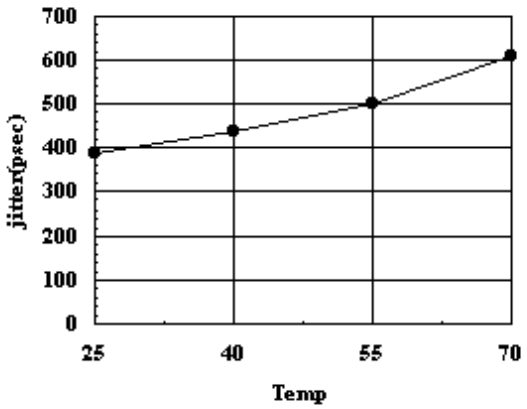

Figure 2. temperature dependence of rms jitter

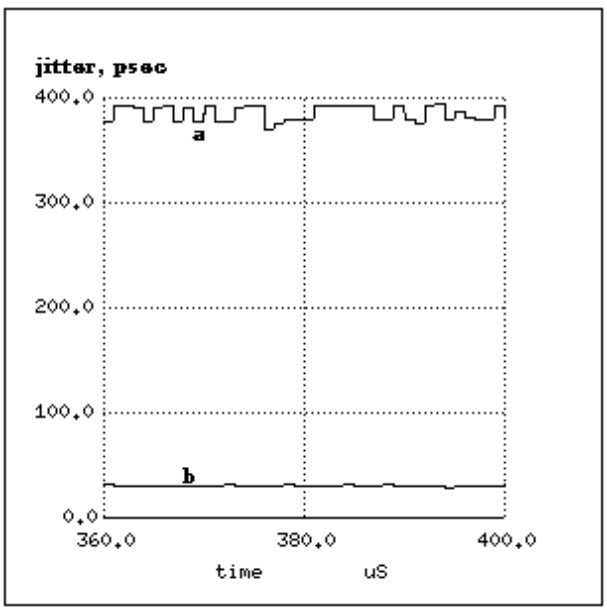

Figure 4. rms jitter for nominal (a) and 10x increased (b) loop bandwidth