Reuse of Existing Resources for Analog BIST of a Switch Capacitor Filter

Érika Cota†, Luigi Carro*, Michel Renovell‡, Marcelo Lubaszewski*, Florence Azaïs‡, Yves Bertrand‡

PPGC† / DELET* – UFRGS
Bento Gonçalves, 9500 Bloco IV
Cx. Postal 15064 91501-970
Porto Alegre – RS – Brazil
{erika,carro,luba}@iee.ufrgs.br

‡ LIRMM UM2
161 Rue Ada
34392 Montpellier Cedex
France
{renovell,azais,bertrand}@lirmm.fr

Abstract

The objective of this paper is to discuss the possibility of reusing the existing hardware originally present in an analog application to implement test functions for a completely autonomous self-testable solution. In this first approach, a 8th analog linear filter is used as an application example. The required modifications in the circuit are presented with the results in terms of area overhead and fault coverage.

1. Introduction

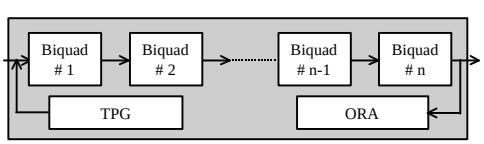
With the advances on analog-digital integrated circuits, faster and more complex test equipment are required to meet ever more severe test specifications. An attractive alternative to simplify the test equipment is to move some or all the tester functions onto the chip itself. The use of Built-In-Self-Test for high volume production of mixed signal ICs is desirable to reduce the cost per chip during production-time testing by the manufacturers. In addition, it helps to perform diagnosis in the field.

In the past few years, many published papers have been concerned with the definition of DFT or BIST techniques [1-8] but few papers are concerned with the implementation of completely autonomous self-test capabilities [1,4,6]. The implementation of completely autonomous self-test capabilities implies the use of on-chip Test Pattern Generators (TPGs) and Output Response Analyzers (ORAs). In case of analog or mixed integrated circuits, two types of TPGs and ORAs can be defined: Modules dedicated to multi-frequency signal and modules dedicated to transient signal. These modules are called 'multi-frequency TPGs or ORAs' and 'transient TPGs or ORAs'.

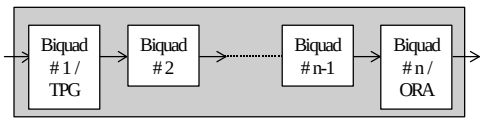
The generated or compacted signal can be analog or digital. Of course, the generation or compaction of a digital signal represents an interesting solution for mixed circuits that originally include digital-to-analog or analog-to-digital converters. This paper deals with purely analog circuits, using purely analog generators or compactors, requiring no conversion. So, considering purely analog modules, some of the authors have published a proposition for a multi-frequency ORA [9] and a transient ORA [10] followed by a proposition for a multi-mode ORA [11]. They also have published a proposition for a multi-mode TPG [12].

In this paper, we use these previously proposed TPG and ORA to implement completely autonomous self-testable solutions for analog filters. The objective and originality of this work is to discuss the possibility of reusing some of the existing blocks originally present in the filter to implement the TPG and ORA. Figure 1.a gives an example of analog filter made of a cascade of basic biquad blocks where the TPG and ORA modules are simply added to the original circuit implying an important additional area. While in figure 1.b, some of the existing biquad blocks are reused in test mode to implement the TPG and ORA implying a very reduced additional area. The study presented in this paper is restricted to multi-frequency TPGs and ORAs but the extension to transient TPGs and ORAs is straightforward.

Section 2 briefly presents the multi-frequency TPG and ORA previously proposed by the authors in [11,12]. Section 3 gives an example of an 8th order filter made as a cascade of 4 biquads and shows how the original biquads are modified in order to implement the TPGs and ORAs. The performances of the approach are presented and discussed in section 4. Finally, section 5 presents our conclusions.



a) Classical BIST implementation



b) Reuse-based BIST
Figure 1: Reuse based BIST

2. Multi-frequency TPGs and ORAs

This section briefly presents a switched-capacitor implementation of multi-frequency TPG and ORA. More details can be found in [14,15] on these modules.

2.1 Multi-frequency TPG

The stimuli generator is a quadrature sine wave oscillator based on two cascaded stages. As shown in figure 2, this oscillator is based on two pure integrators connected in a ring configuration. A 360° phase shift is ensured because the first integrator is inverting, and the second one is non-inverting thanks to the negative resistor in its input. A negative switched-capacitor resistor is implemented by swapping two clock phases (ϕ_1 and ϕ_2, in figure 2) of a positive switched-resistor. The predictable non-idealities of this circuit should ensure its instability [11].

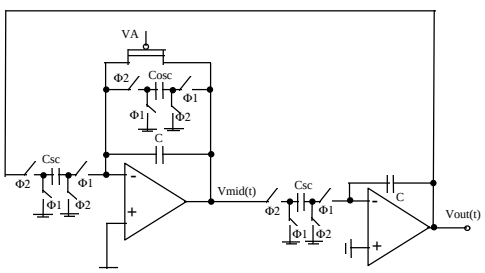


Figure 2: A multi-frequency TPG

Considering the switched-capacitor implementation in figure 2, the frequency of oscillation depends linearly on the frequency of the switching clock (f_{CK}). Since the value of the switched-capacitor resistors in the oscillator is given by $R=1/f_{CK}.C_{SC}$, where ϕ_1 and ϕ_2 correspond to the two phases of f_{CK}, an oscillation frequency of $f_{OSC}=f_{CK}C_{SC}/2\pi C$ is obtained. For instance, if $C/C_{SC}=10$, then a good sampling for the generated signal can be achieved.

The negative switched-capacitor resistor in the local feedback of the first integrator results in a positive feedback which ensures circuit instability and a faster growth in the amplitude of the oscillations. Additionally, voltage limitation preserving signal symmetry is achieved by using a MOS transistor in parallel with the local feedback branch of the first integrator. The bias voltage V_A is used to adjust the amplitude of oscillation.

2.2. Multi-frequency ORA

The output response analyzer is also based on a cascade of two integrators. As shown in figure 3, this signature analyzer is based on a double integrator and a comparator. A digital signature is obtained by computing the time for the output of the second integrator to reach a predefined reference voltage (V_{REF}). If a counter is used for computing digital signatures, counting must be enabled from the integration start up to the time when the comparator output goes high.

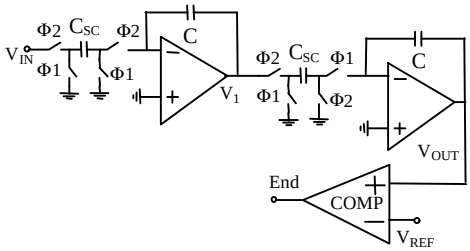


Figure 3: A multi-frequency ORA

[9] presents the mathematical prove of this system as an ORA. Figure 4 shows the effect of the integration of a signal with V_0=1V and f=500Hz, with a time constant $\tau=8.10^{-4}$s. Ideal operational amplifiers are considered. Due to the initial condition $V_{C|t=0}=0$, the first integration results in a signal shifted above analog ground according to (1). The second integration gives an increasing (monotonically) value for V_{OUT}.

It is clear that a maximum integration time T_{max} must exist since some signals may require excessively long times and lead to time counting overflows. Those signals

f(t) for which $\frac{1}{t^2}\int_0^{T_{max}}\int_0^t f(t).dt < V_{REF}$,$V_{C|t=0}=0$ (1)

do not reach the threshold V_{REF} before T_{max}. This will therefore result in a signature that does not represent the signal. T_{max} and V_{REF} limit then the input space of signals, together with the time constant τ. Smaller values of τ increase the input valid space. In practice, since a valid input space cannot be ensured for a faulty circuit, counter overflows should automatically disable counting in order to avoid signature aliasing.

3. Reuse-based Analog BIST

This section is dedicated to the presentation of the reused-based analog BIST technique we propose using as example an 8th order low-pass filter.

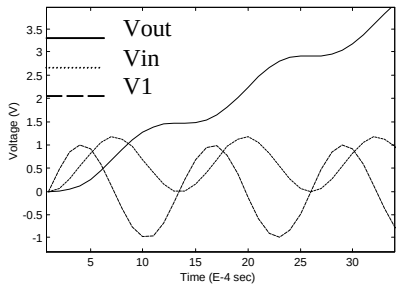
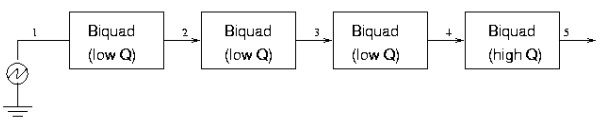


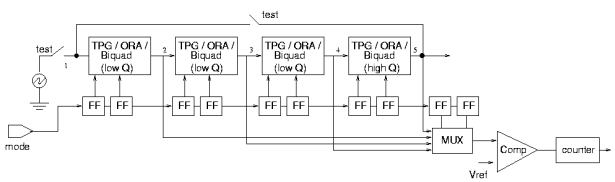
Figure 4. Signature for V_0=1V, f=0.5kHz and τ=0.8ms

3.1. The 8th analog filter

In the analog world, it is common to use a cascade of basic biquad blocks in order to built a filter of greater order [13]. This is the case, for example, of the 8th low-pass filter presented in figure 5.a made of 4 cascaded biquads. This filter has a cutoff frequency of 1.36KHz and the Q values for its biquads are, respectively, 0.51, 0.6, 0.9, and 2.56. The biquads are implemented with switched capacitors controlled by a 1MHz clock signal. The topology of the first three low Q biquads is presented in figure 6.a, while figure 6.b shows the topology of the last biquad with high Q [13].



a) original filter topology

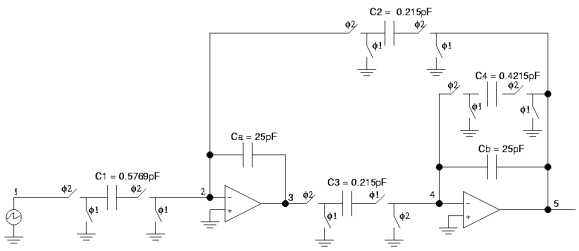


b) self-testable filter topology

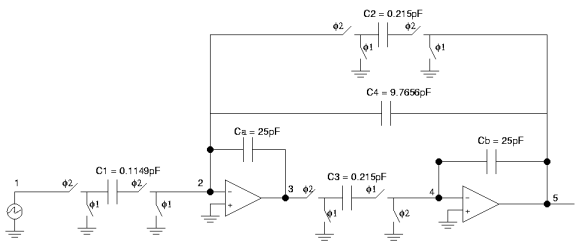
Figure 5: The 8th order low pass filter

3.2. Reuse-based BIST of the 8th order filter

Figure 5.b shows the new implementation of the filter given in figure 5.a with self-test facilities. Each biquad in the filter is modified in order to implement the TPG and the ORA revised in section 2. As shown in figure 7.a and 7.b, the modification of the low Q biquad requires the addition of only 4 extra switches and the modification of the high Q biquad only 5 extra switches. Because the ORA of figure 3 is built with 2 OPAMPS plus a comparator, while the original biquad in the filter has only 2 OPAMPS, it should be necessary to add a comparator to each original biquad. In order to save silicon area, only one comparator is added to the whole circuit and connected to each biquad output through a multiplexer (figure 5.b).



a) Low Q biquad topology

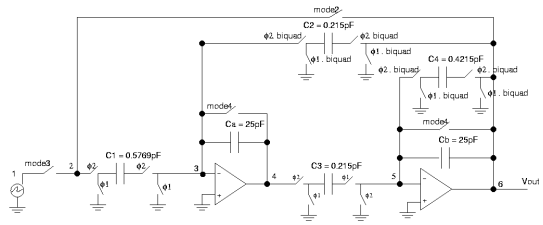


b) High Q biquad topology

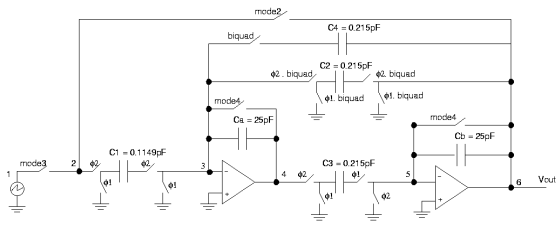
Figure 6: Original biquad topology

With those modifications, each block is able to perform its nominal function (mode biquad) or to work as a sinewave generator (mode2) or as a signature analyzer (mode3). Besides, both integrators can be reset by shorting their integration capacitors (mode4). The operating mode of a given biquad is determined by two configuration bits stored in two flip-flops. Figure 5.b shows that a filter including n cascaded biquads requires 2n configuration bits plus $\log_2 n$ bits to control the multiplexer. These $2n+\log_2 n$ flip-flops are serially connected to form a shift register which is loaded with the desired configuration.

Knowing that each biquad is able to generate test stimuli and analyze output responses, the test procedure presented in figure 8 can now be used for the 8th order filter. The test procedure includes 4 phases, each phase being dedicated to the test of one of the biquads. As an example of operation, in the first phase the second biquad is tested, having the first one as TPG and the third one as ORA (figure 8.a). Then, in the second phase, the test functions are 'moved' to the next blocks so that the third block is tested (figure 8.b), with the second biquad as TPG and the fourth one as ORA. The test of the fourth block in the third phase is presented in figure 8.c. In this case, the switch connecting the output to the input of the first biquad is 'ON', so that the first block can analyze the response of the fourth biquad. Finally, in phase 4, the first biquad can be tested if the fourth block is used as TPG and the second one as ORA (figure 8.d).



(a) Low Q biquad/TPG/ORA topology



(b) High Q biquad/TPG/ORA topology

Figure 7: New biquads topology

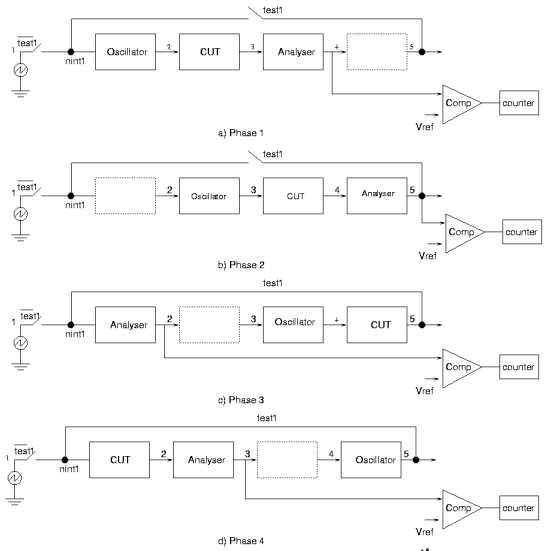


Figure 8: Test sequence for the 8th order filter

4. Performances of the reuse-based BIST

The reuse-based BIST technique we propose must be now evaluated using the classical criteria of area overhead, circuit performance degradation and fault coverage.

4.1. Area overhead

In this test scheme, the 2 existing OPAMPs of each biquad with its surrounding capacitors and switches are reused to allow the transformation of the original biquad in TPG or ORA. We finally observe that the proposed scheme only requires the addition of:

- 4 or 5 switches per biquad;
- A 4 input-multiplexer, a comparator;
- 2 logic gates for the Φ1.biquad and Φ2.biquad signals;
- 1 counter to measure the signature time.

The cost in terms of additional area of this BIST solution consists only on this small circuitry, being extremely low.

4.2. Performance degradation

The 8th filter was simulated with the modified biquads presented above. Figure 9 shows a comparison of the behavior of the original biquad (black curve) and the modified one (gray curve), around the biquad corner frequency (1.36KHz). As it can be seen, the difference between both curves is very acceptable.

4.3. Fault coverage

In this work, the goal is to perform the test functions only with the original components of the circuit in order to have a minimum silicon overhead. It is important to notice that the original biquads have values for their internal components that have obviously been determined according to the circuit specifications, not for test purposes. This way, amplitude and frequency of the sinewave generated by the TPG are determined by the component values of each biquad. The same occurs for the sensitivity of the ORA and the time it takes to achieve the voltage reference. Consequently, the test qualities of these TPG and ORA obtained from the existing blocks must now be evaluated with regards to fault detection.

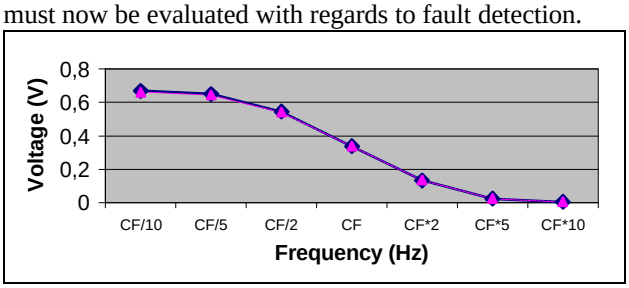


Figure 9: Frequency response for the original (black curve) and the self-testable biquad (gray curve)

Table 1 shows the characteristics of the sinewave signal generated by each biquad and the fault free signature obtained for each phase of figure 8.

In order to perform the fault coverage analysis, the test procedure presented in figure 8 is applied, and faults are injected in the biquads. A total of 36 soft and hard faults are injected in each biquad:

- ±10% small deviation on each component (12 faults),

- ±50% large deviation on each component (12 faults),
- Hard short and open on each component (12 faults).

Table 1: Biquad test characteristics

Biquad #	Frequency Hz	Amplitude V	Signature µs
1	2257	7.18	302
2	2061	6.57	246
3	1689	5.28	351
4	999	3.03	511

Table 2: Fault coverage

Biquad #	Detection Rate
1	97,2%
2	97,2%
3	97,2%
4	94,4%

In order to account for the normal technological deviations, we consider a fault as detected when a difference of at least 1 pulse appears in the counter that measures the signature. Table 2 shows the fault coverage obtained for each biquad. From table 2, very good fault coverages ranging from 94% to 97% appear making the proposed BIST scheme very efficient in term of fault detection. The hard short and open faults are all detected as well as the soft faults corresponding to large deviation. All the soft faults corresponding to small deviations are detected, with one exception, for the 97,2% coverage and 2 exceptions for the 94,4% coverage. A small deviation of +10% in capacitor C2 of biquad 1,2 and 3 causes a variation in the signature analyzer that is in the limit of detection. In the last biquad, the same occurs for a +10% deviation in C4. These faults were considered undetected, since they may change, or not, the counter result.

Despite of this good fault coverage, it is possible to try to detected these few non detected faults. We observed that the undetected faults are detected if we consider the output of the biquad under test and not the output of the ORA. This point clearly indicates that the ORA and not the TPG is responsible for this small aliasing. Techniques are now under development to change the sensitivity of the ORA by modifying, in equation (2), either f_{CK} (the clock frequency) or C_{SC}, the capacitor.

5. Conclusion and Discussion

This paper discusses the possibility of reusing the existing hardware originally present in an analog circuit to implement test functions for a completely autonomous self-testable solution. The proposed reuse-based BIST technique is illustrated with an example of 8^{th} analog linear filter. It is shown that the area overhead only consists of a few switches, logic gates, a comparator and a counter. The impact on the filter performances is reasonable and the approach has shown itself efficient in terms of fault coverage.

The proposed testing method can be used for high order filters and for different applications, as for stereo-audio with anti-alias filters and sigma-delta integrators for audio applications.

6. References

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