# An on Chip ADC Test Structure*

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## Abstract

*In this paper, a new built-in self-test structure to test the static specifications of analog to digital converters (ADCs) is presented. A ramp signal generated by an integrator serves as a test input signal. A specific range of this signal is divided into $2^{n+1}$ segments, with each segment corresponding to one output combination of an n+1-bit counter, where n is the number of bits of the ADCs under test. The testing process is done with digital data processing by comparing the outputs of ADCs under test with the outputs of the n+1-bit counter. Simple structure, low area overhead, and high speed are the advantages of the proposed test structure.*

## 1. Introduction

Previously several approaches or systems have been developed for ADC testing [1, 2, 3, 4, 5, 6, 7]. An analytic approach to testing a set of parameters for ADCs based on Walsh functions is proposed in [1]. Another method proposed in [2] employs Wavelet transforms to measure the ADC errors including nonlinearity, gain error, and offset error. The analytic approaches in [1, 2] require a computing core for their complex computation when the system is integrated on a chip.

In [3] a sinewave generator and some processing core circuits are incorporated into a VXI bus-based system to test ADCs. This system can perform both static and dynamic testing, but it requires large chip area when they are implemented on a chip. In [4] a similar system is set up with external instruments and two methods for measuring the total harmonic distortion of an A/D converter are developed. A large amount of sampled data must be collected to support these two methods. Two built-in self-test (BIST) structures for DACs are respectively presented in [5] and [6]. These BIST structures can be extended to test only DAC-based ADCs. Furthermore, multiple level DC reference voltages are required and many switches for creating signal paths are employed. A BIST methodology is proposed for ADCs by simple digital functions [7]. The linearity of the ADCs, however, is tested by monitoring the LSB externally.

In this paper, we present an on-chip BIST structure for ADCs. The basic idea is to use a transconductor-based integrator to generate a high performance ramp signal as the test stimulus. This ramp signal is synchronized with the outputs of an *n*+1-bit counter, where *n* is the bit number of the ADC under test. More specifically, we divide a specific range of the ramp signal into $2^{n+1}$ segments. Each segment corresponds to one output combination of the *n*+1-bit counter. Thus, the counter outputs can be used as the references in the testing phase. The test responses are analyzed by comparing the outputs of the ADC with those of the *n*+1-bit counter whenever a transition occurs at the output of the ADC. Offset error, gain error, all *INL* and all *DNL* can be tested by some simple digital circuits. Thus the advantages of our BIST structure include the simplicity in design methodology, the digital process of test responses and the high speed in test execution.

## 2 Specifications of ADCs

Refer to Figure 1, each digital output code of the ADC lies between two transitions. The real and ideal voltages at the transition from the output code *k-1* to *k* are represented by $V_{rtran}(k)$ and $V_{itran}(k)$ respectively. $V_{rtran}(1)$ and $V_{rtran}(2^n - 1)$ are called the lowest and highest transitions of the real transfer function. $V_{rmed}(k)$=$\frac{V_{rtran}(k)+V_{rtran}(k+1)}{2}$ is the analog voltage that lies halfway between the two bounding transitions of the real transfer function. $V_{imed}(k)$ has a similar definition as $V_{rmed}(k)$ for the ideal transfer function. $V_{il}$ and $V_{ih}$ are the specified lower and upper bounds of the input signal that the ADC can operate. $V_{irang}$(*nLSB*) represents the amount of input voltage in a range *nLSB* at the ideal transfer function. For example, $V_{irang}$(*kLSB*)=$\frac{V_{ih}-V_{il}}{2^n}\times k$. We set

*This work was supported by the National Science Council of R.O.C., under contract NSC-88-2215-E-006-023.

$V_{itran}(k)$=$V_{il} + V_{irang}((k - \frac{1}{2})LSB)$ [8].

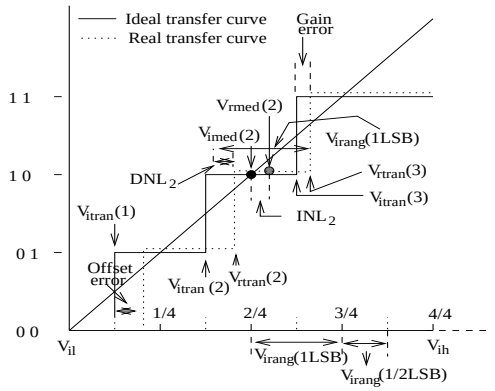


**Figure 1. The illustration of specifications of an ADC.**

Integral nonlinearity (*INL*): is the difference of the analog input voltage $V_{rmed}(k)$ from $V_{imed}(k)$, or $INL_k$=$V_{rmed}(k)-V_{imed}(k)$ . For example, in Figure 1, $INL_2$ is shown.

Differential linearity (*DNL*): is the difference of the analog input range corresponding to the same input code *k* from $V_{irang}$(1LSB), or $DNL_k = V_{rtran}(k + 1)-V_{rtran}(k)-V_{irang}$(1LSB). Figure 1 shows an example of $DNL_2$.

Gain error ($V_{gain}$): is the difference between the real and ideal voltages at the highest transition from the output code $2^n-2$ to $2^n-1$, or $V_{gain}$=$V_{rtran}(2^n-1)-V_{itran}(2^n-1)$.

Offset error ($V_{offset}$): is the difference between the real and ideal voltages at the lowest transition from the output code 0 to 1, or $V_{offset}$=$V_{rtran}(1) - V_{itran}(1)$.

## 3 Test Structure

The block diagram of the test structure is shown in Figure 2. It consists of the following components.

(1). An ADC: th circuit under test (CUT).

(2). An input test pattern generator: It produces a ramp test signal $V_{ts}$ whose specific range from $V_{il}$ to $V_{ih}$ is divided into $2^{n+1}$ segments and each segment corresponds to one output code of an *n*+1-bit counter. The slope of the output voltage is controlled by $V_{gm}$. The initial voltage is set by the $V_{init}$ pin to guarantee that $V_{il}$ can be precisely synchronized with the start of a proper initial state.

(3). An *n*+1-bit counter: The counter outputs serve as the references of the test response analyzer when the ramp signal is synchronized with the counter outputs. The clock frequency (*f*) of the counter is set to $2 * f_{oper}$, where $f_{oper}$ is the operational frequency of the ADC on a chip.

(4). A test response analyzer: It consists of a transition detector, a *DNL* detector, an *INL* detector and an *n*-bit counter.

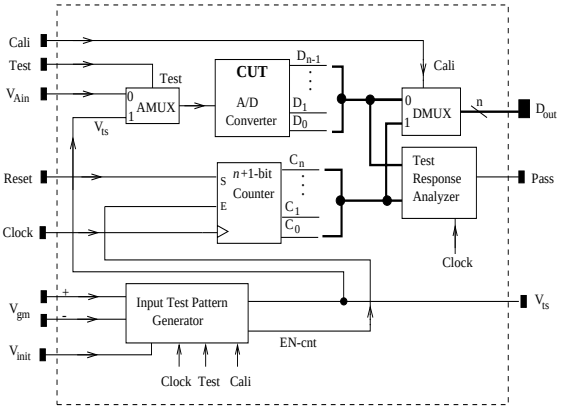


**Figure 2. The ADC test structure.**

The *INL* detector also performs the offset error and gain error detections at the lowest and highest transitions.

(5). An analog and an *n*-bit digital multiplexers: They are used to create signal paths for either normal or test operations.

## 4 Calibration and Test Procedures

Figure 3 shows the circuit block diagram of the input test pattern generator which contains a linear differential integrator and a voltage window comparator/chopper. When the signal *Test* or *Cali* is active, the signal *Inte* is activated at the rising edge of the clock signal to start the integration.

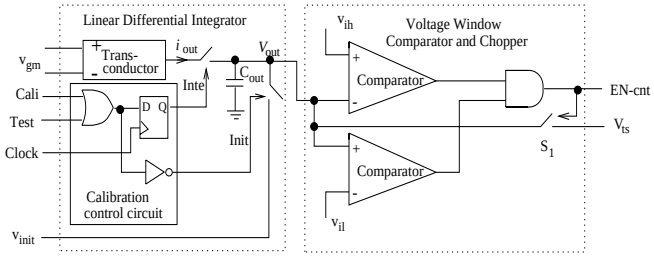


**Figure 3. The analog input test pattern generator.**

When the signal $V_{out}$ is between the lower bound voltage $V_{il}$ and upper bound voltage $V_{ih}$, *EN-cnt* is set to 1 and $S_1$ is on to supply $V_{ts}$ as an input test pattern. The ideal values of $V_{gm}$ and $V_{init}$ can be estimated from the transfer function of the integrator.

$\triangle V = \int_0^T \frac{i_{out}}{C_{out}} dt = \int_0^T \frac{g_m V_{gm}}{C_{out}} dt = \frac{g_m V_{gm}}{C_{out}} T$

where $g_m$ and $C_{out}$ are the known parameters of the transconductance and the embedded capacitance of the integrator, $\triangle$V=$V_{ih} - V_{il}$, and $V_{gm}$ and T can be predefinded for system requirements. For example, when the sampling frequency $f_{oper}$ of a 11-bit ADC is 0.5M*Hz*, the clock frequency of the 12-bit counter is defined to 1M*Hz*, two times $f_{oper}$. The time of the integration from $V_{il}$ to $V_{ih}$ is then defined as $2^{12} \times 10^{-6}$ seconds. Hence

$V_{gm}$=$\frac{C_{out}\triangle V}{g_m(4096u)}$

For the the output voltage $V_{out}$=△V+$V_{init}$ at capacitor $C_{out}$, the $V_{init}$ can be obtained through calibration processes to ensure that $V_{out}$ at $V_{il}$ and $V_{ih}$ are synchronized to the rising edge of the proper counter outputs.

Figure 4 shows the demonstration of the calibration. The starting time of the active *EN-cnt* signal is slightly later than the time of the integrator output voltage at $V_{il}$ such that the counter can count up at the next positive edge of the clock signal. The initial value of the counter in Figure 4 is 2 which will be explained in the next section.

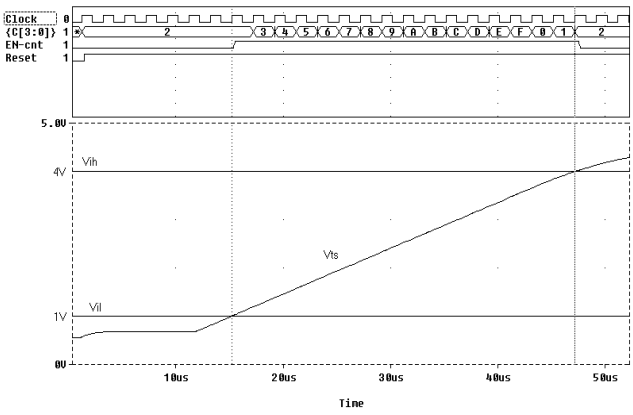


**Figure 4. The calibration for the synchronization between the integrator and counter.**

The purpose of the calibration is also to provide the cancellation of component deviations in manufacture processes. If the integration time has deviation from the defined value, a fine adjustment in $V_{gm}$ or clock frequency can be applied to rearch the synchronization. Figure 5 shows an example of synchronization of a test signal to a 3-bit counter for a 2-bit ADC. The signal from $V_{il}$ to $V_{ih}$ is synchronized with the outputs of the 3-bit counter from 0 to 7.

The test procedure can be started, after the correct correspondence between $V_{ts}$ and the counter outputs is identified. The test procedures proceed as follows:

1. Set clock frequency $f = 2 * f_{oper}$ for the counter.
2. Set *Cali*=*Test*=0 such that $C_{out}$ is connected to $V_{init}$.
3. Provide $V_{init}$ and $V_{gm}$ obtained from the calibration.
4. Set *Cali*=0 and *Test*=1 to start the integration and the $V_{ts}$ is connected to the input of the ADC through the AMUX.
5. When the output of the integrator reaches the value of $V_{il}$, *EN-cnt* is automatically set to 1 and the counter starts to count and $V_{ts}$ is converted by the ADC.
6. Whenever a transition appears at the output of the ADC, the responses of the ADC are analyzed.
7. The offset error, gain error, and *INL* are analyzed by the *INL* detector, and the *DNL* is tested by the *DNL* detector. When all specifications are within acceptable ranges, *Pass* is 1. Otherwise, *Pass*=0 when a fault appears.

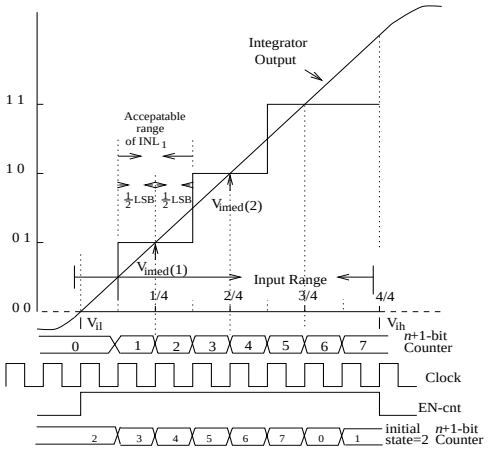


**Figure 5. The diagram to indicate the ramp input test signal referred to an *n*+1-bit counter and acceptable range of *INL*.**

## 5 Analog Input Test Pattern Generator

The input analog signal pattern generator includes a differential linear integrator and a voltage window comparator/chopper as shown in Figure 3. The integrator is the main element for this proposed structure whose linearity dominates the quality of the test structure. It can be realized by a OTA-C (Operational Transconductance Amplifier and Capacitor) with a folded cascode structure [9, 10, 11]. In addition, with current convery compensation techniques [12] and phase compensation techniques [13], a high linear ramp signal which is trimmed by the window comparator/chopper can be obtained. When the ramp signal is between the lower bound voltage $V_{il}$ and upper bound voltage $V_{ih}$, the *EN-cnt* is set to 1 and $S_1$ is on to supply $V_{ts}$ as an input test pattern (Refer to Figure 3).

## 6 Test response Analyzer

Figure 6(a) shows the test response analyzer which examines the ADC outputs to determine whether they are within the acceptable ranges.

Let $D_{n-1}..D_0$ be the output code of the ADC where $D_0$ is the least significant bit. The output transition detection for the ADC can be achieved by monitoring only the least significant bit as shown in Figure 6(b). When a transition (either 1→0 or 0→1) at $D_0$ enters the transition detector, a pulse with narrow active width is generated as a transition pulse named *Tran*.

After considering the absolute accuracy $\pm\frac{1}{2}$LSB, the acceptable input range for producing output code 01 is from $V_{imed}(1)$-$V_{irang}(\frac{1}{2}LSB)$ to $V_{imed}(1)$+$V_{irang}(\frac{1}{2}LSB)$ as shown in Figure 5. On the other hand, the

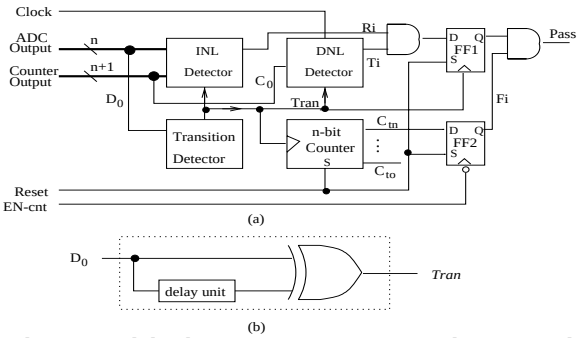


**Figure 6. (a) The test response analyzer, and (b) the transition detector.**

transition from 0 to 1 of the ADC output occurs at $V_{ts}$=$V_{il}$+$V_{irang}$($\frac{1}{2}LSB$). Considering the absolute accuracy $\pm\frac{1}{2}LSB$, an acceptable transition locates the range between $V_{il}$ and $V_{il}$+$V_{irang}$(1*LSB*). The corresponding outputs of the counter would be 000 and 001 if the initial state of the counter is 0. Since the comparison between the outputs of the ADC and the counter is made right after the transition, the current output of the ADC is 01 at this moment.

**Table 1. (a) The acceptable range of the transition for *INL*, and (b) the unacceptable range of *DNL***

| Transitions | ADC output after transition | Counter output | Spec. |
|---|---|---|---|
| 0 → 1 | 0 1 | 0 1 0<br>0 1 1 | Offset error, *INL* |
| 1 → 2 | 1 0 | 1 0 0<br>1 0 1 | *INL* |
| 2 → 3 | 1 1 | 1 1 0<br>1 1 1 | Gain error, *INL* |

(a)

| | *DNL* > 3/2 *LSB* | | *DNL* < 1/2 *LSB* | |
|---|---|---|---|---|
| ADC output transition | Counter output | Clock state | Counter output | Clock state |
| 1 → 2 | 1 0[0] | 1 | 1 0[1] | 0 |
| 2 → 3 | 1 1[1] | 0 | 1 1[0] | 1 |

(b)

In order to simplify the circuit of the *INL* detector, the counter is set to have an initial value 2. The details of the corresponding counter outputs for each 2-bit ADC output are described in Table 1(a). It can be seen that if we take the *n* most significant output bits of the *n*+1-bit counter without the least significant bit ($C_0$) as a reference, then the *INL* detector can be designed by simply comparing between them. Figure 7(a) shows the circuit of the *INL* detector. These operations are done at the active period of the signal *Tran*. When the *INL* is acceptable, the signal *Ri*=1. Otherwise, *Ri*=0. When some faults such as missing codes, stuck at 0 or stuck at 1 at the $D_0$ bit occurs, some or all *INL* detections will be skipped. There are $2^{n-1}$ transitions 0→1 at $D_0$ bit, if it has normal outputs. The *n*-bit counter shown in Figure 6(a) is used to count the number of the transitions. The $C_{tn}$ bit changes from 0 to 1 when $D_0$ bit completes $2^{n-1}$ transitions 0→1. The initial output Q of the FF2 is set to 1. *EN-cnt* is 1, when $V_{ts}$ locates between $V_{il}$ and $V_{ih}$. After $D_0$ bit has $2^{n-1}$ transitions 0→1 and *EN-cnt*=0 for $V_{ts}$ is over the $V_{ih}$, $F_i$ keeps at 1. Otherwise, if the transitions of $D_0$ bit is less than $2^{n-1}$, $F_i$ changes to 0.

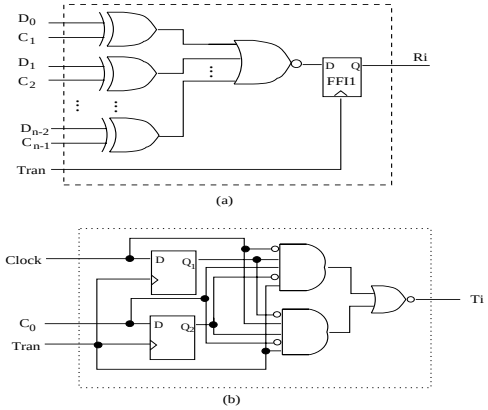


**Figure 7. (a) The *INL*, and (b) *DNL* detectors.**

The ideal difference for adjacent ADC outputs in an analog input signal is $V_{irang}$(1LSB). The accepatable difference is from $V_{irang}$ ($\frac{1}{2}LSB$) to $V_{irang}$($\frac{3}{2}LSB$) when the absolute accuracy $\pm\frac{1}{2}$LSB is considered. In Table 1(a), it is known that the acceptable range of the transition from 1 to 2 corresponds to 100 or 101 of the counter outputs to meet the requirement of *INL*. Hence when there is no *INL* error, the 1→2 transition may occur between $V_{imed}$(1) and $V_{imed}$(2).

We can simply design the *DNL* detector by detecting the unacceptable range. Figure 8 shows the two kinds of certainly unacceptable range between the 1→2 and 2→3 transitions. If the 1→2 transition occurs at the range **TR1** (counter=4, clock=1), the range **TR2** (counter=7, clock=0) for the 2→3 transition is accepted by *INL* testing but not by *DNL* testing because the difference between **TR1** and **TR2** is over the maximum range $\frac{3}{2}LSB$. If the 1→2 transition occurs at the range **TR3** (counter=5, clock=0), the 2→3 transition at the range **TR4** (counter=6, clock=1) is not acceptable because the difference between two transitions is less than $\frac{1}{2}LSB$.

We conclude this relation in terms of the counter outputs and the states of the clock signal in Table 1(b). We find that we only need to monitor the least significant bit $D_0$ and the state of the clock signal for *DNL* testing, and intuitively the *DNL* detector depicted in Figure 7(b) can do this job. The two most significant bits are used for the *INL* test.

The *Pass* signal is in terms of *Ti*, *Ri* and *Fi*. If one of *Ti* and *Ri* is 0, then *Pass* is also 0 to indicate the failure of the ADC test. Finally $2^{n-1}$ transitions are checked. If it

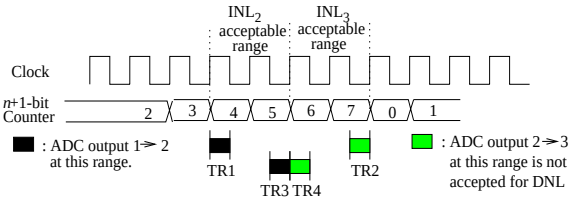


**Figure 8. The unacceptable ranges for *DNL* testing between two adjacent transitions.**

does not complete, *Pass*=0. We realize the differential input integrator with a folded cascode operational transconductance amplifier (OTA) and a capacitor (3p). A second generation current conveyor (CCII) compensation is applied to improve the precision of linearity [12]. Figure 9 shows the simulation results for a 11-bit ADC implemented with behavior models by ISpice. An *INL* and a *DNL* faults which occur at the outputs 009H and 7F3H are detected, respectively. Figure 9 (a) and (b) are the expanded waveforms near the faults for easy observations.

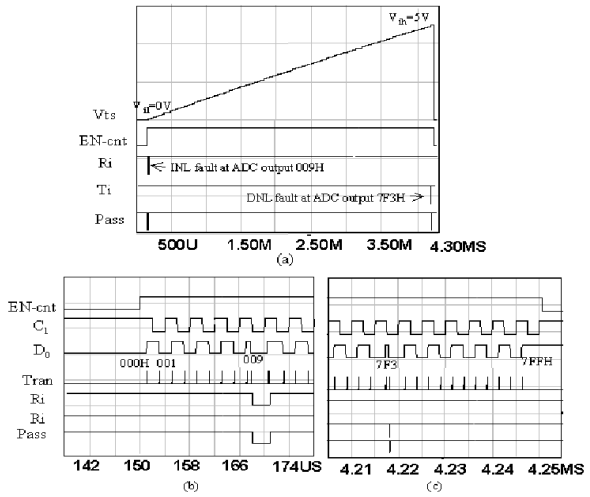


**Figure 9. The waveforms for demonstrating the detection of the 11-bit ADC.**

## 7 Conclusions

A simple and efficient test structure on a chip for testing ADCs is proposed. A high performance linear integrator is used to supply a test signal which is synchronized with the output of an $n$+1-bit counter. The testing of ADCs is achieved in digital processes. The test response analyzer is relatively simple based on the detailed analysis of the relations between the outputs of the ADC and the counter. From the calibration process, the errors from the mismatch of the components can be corrected. The testing is completed in $2^{n+1}$ clock cycles. Finally we would like to point out that the effectiveness of this BIST structure is highly dependent on the performance of the integrator and the synchronization between the outputs of the integrator and the counter. We believe that this structure will work well for low-bit ADCs testing. For high-bit ADCs, very high performance integrators would be needed and a tradeoff between the cost of the integrators and the accuracy that can be achieved has to be made.

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