# A BIST Scheme for On-Chip ADC and DAC Testing

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## Abstract

*In this paper, we present a BIST scheme for testing on-chip AD and DA converters. We discuss on-chip generation of linear ramps as test stimuli, and propose techniques for measuring the DNL and INL of the converters. We validate the scheme with software simulation—5% LSB (least significant bit) test accuracy can be achieved in the presence of reasonable analog imperfection.*

## 1 Introduction

Testing the analog/mixed-signal circuitry of a mixed-signal IC has become a difficult task. The main challenges originate from the fact that most analog/mixed-signal circuits are tested by functionality, which is both expensive and time-consuming. To resolve the problem, one promising strategy is the the built-in self-test (BIST) approach in which both stimulus generation and measurements are performed on-chip. In this work, we focus on an efficient BIST scheme for testing on-chip AD and DA converters.

Recently, several BIST schemes for DA and AD converters were proposed. In [1], the authors utilize the on-chip delta-sigma DAC for sine wave generation and digital signal processing (DSP) techniques for data analysis. However, the technique needs both on-chip ADC and DAC, and intensive computation, which is not always possible. The BIST approach reported in [2] relies on analog circuitry and reference voltages for measurements, which makes it vulnerable to analog imperfections. The oscillation-test method proposed in [3] does not need functional test stimuli. Nevertheless, it is not clear the impact of the control logic delay and the imperfect analog BIST circuitry on the test accuracy. The work in [4] proposes an efficient polynomial fitting algorithm for DAC and ADC BIST. The transfer map of a converter is fitted to a polynomial from which various parameters like offset, gain, and harmonic distortion can be derived. The drawback is again the need of both on-chip ADC and DAC. In [5], the authors propose a BIST methodology for testing AD converters, which is intended to reduce the number of the ADC output bits that have to be monitored externally. In [6], a BIST design of current-mode algorithmic ADC is proposed. The methodology cannot be used for testing other kinds of ADC's.

The proposed BIST scheme in this work employs the delta-sigma modulation technique [7] to generate the required linear ramp for testing the converters. Since we do not rely on the on-chip AD and DA converters for stimulus generation and data conversion, our BIST strategy does not require the existence of both on-chip AD and DA converters, which makes it feasible for most mixed-signal IC's.

For ADC testing, we use the proposed BIST strategy to perform the "linear histogram testing" ([8]) and measure differential/integral non-linearities (DNL/INL). For DAC testing, we propose a test scheme that employs an analog comparator and two counters for measuring the DAC parameters. The DAC BIST strategy is immune from the common offset voltage of the analog comparator since it is canceled out in the analysis process and thus has little effect on the test accuracy.

We demonstrate how the test stimulus, i.e., a linear ramp, that can achieve the desired test accuracy is generated, and perform a series of software simulation to show that the stimulus quality has high tolerance to analog variation. Measurements of DNL and INL for DA and AD converters are also implemented in software—a measurement accuracy of 5% LSB can be achieved in the presence of reasonable analog imperfections.

In Section 2, we give an overview of the delta-sigma modulation technique, and DAC/ADC testing. In Section 3, we illustrate the proposed BIST architecture and the test procedures for the converters. Section 4 discusses the issues of generating the linear ramp suitable for our BIST scheme. Simulation results are shown in Section 5 to validate our ideas. We then conclude the work in Section 6.

## 2 Preliminaries

### 2.1 Delta-Sigma modulation based signal generation

For on-chip test stimulus generation, we use the delta-sigma modulation based approach proposed in [7]. A *software* delta-sigma modulator converts the desired signal to a one-bit digital stream. The digital 1's and 0's are then transferred to two discrete analog levels by a one-bit DAC

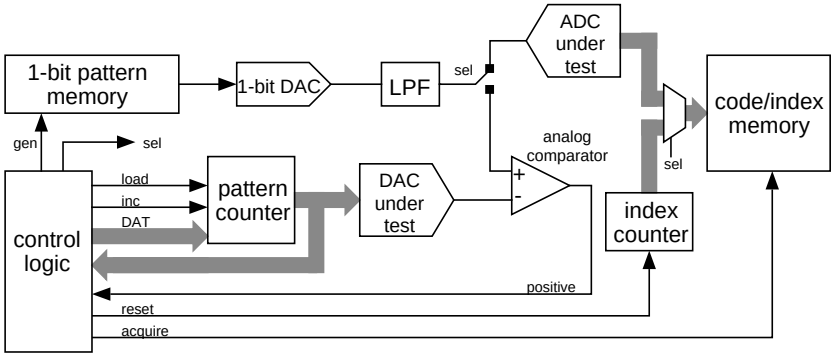


**Figure 1. The BIST scheme.**

followed by a low-pass filter which removes the out-of-band high-frequency modulation noise, and thus restores the original waveform. In practice, one extracts a segment from the delta-sigma output bit stream that contains an integer number of signal periods. The extracted pattern is stored in on-chip memory, and periodically applied to the the one-bit DAC and low-pass filter to generate the desired stimulus.

### 2.2 The converter parameters

In this work, we are interested in measuring the non-linearities, i.e., DNL and INL, of the converters. For a DAC, INL indicates the deviation of actual output values from the ideal straight I/O curve, and DNL is a measure of the irregularity or non-uniformity in the increments of its output voltage or current.

Unlike the DAC, the ADC has a discrete output set but a fuzzy input, a continuum of input voltage for each output code. The edges of the fuzzy input segments (or decision levels) are only statistical quantities, i.e., the most possible values at the existence of dynamic error and noise. One can adapt most of the DAC parameters to those for ADC—the voltage levels produced by a DAC are analogous to code centers (the centers of the fuzzy input steps) in an ADC. However, the definition of DNL is different. If the decision levels are known, one can compute the statistical step width for each output code and subtract the average step size to obtain the DNL value.

### 2.3 The linear histogram testing

For ADC testing, we use the "Linear Histogram Testing" approach. The analog input is a linear ramp that covers the full-scale range (FSR) of the ADC, and the outputs of the ADC are analyzed to create the Tally and Weight arrays (more details can be found in [8].)

Assume that the ADC is an $n$-bit one, and its output codes are $c_0, c_1, \ldots, c_{2^n-1}$. The Tally array, denoted by $T$, has $2^n - 2$ elements corresponding to $c_1, c_2, \ldots, c_{2^n-2}$ (the tallies for code $c_0$ and $c_{2^n-1}$ are not valid because their input ranges are not doubly bounded,) and $T\,(i)$ is the number of occurrences of output code $c_i$. The average step width, which corresponds to 1 LSB, is

$$\overline{w} = \frac{\sum_{i=1\cdots 2^n-2} T\,(i)}{2^n - 2}$$

and one can obtain the differential and integral non-linearity (as fraction of 1 LSB):

$$\begin{aligned} \mathrm{DNL}_i &= (T\,(i) - \overline{w})\,/\overline{w} \\ \mathrm{INL}_i &= \begin{cases} 0 & \text{if } i = 0 \\ \mathrm{INL}_{i-1} + (\mathrm{DNL}_i + \mathrm{DNL}_{i-1})\,/2 & \text{otherwise} \end{cases} \end{aligned}$$

## 3 The BIST scheme

The overall BIST structure for the proposed ADC/DAC BIST scheme is depicted in Fig. 1. The required functional blocks and control signals are as follows:

*1-bit pattern memory* stores the delta-sigma modulated one-bit digital stream for generating a linear ramp. When activated (by $gen$), its contents are periodically applied to the 1-bit DAC.

*1-bit DAC* transfers the digital values (1's and 0's) to two discrete analog levels.

*LPF* is a low-pass filter that removes the out-of-band modulation noise and thus restores the desired linear ramp.

The *pattern counter* generates the desired input codes for the DAC under test. The $load$ signal loads the counter with $DAT$, and the $inc$ signal increments its contents.

The *analog comparator* outputs 1/0 if the the analog quantity in the positive end is greater/less than that in the negative end.

The *index counter* is reset by the $reset$ signal and incremented in each clock cycle.

The *code/index memory* acquires and stores the ADC output code or the index counter value when the $acquire$ signal is high. The collected data are then analyzed to make the pass/fail decision.

*sel* directs the output of the LPF to the desired block (the ADC under test or the analog comparator), and selects the input source for the code/index memory (from the ADC under test or the index counter.)

Note that Fig. 1 shows the BIST structure for testing *both* DAC and ADC. The two counters, and the analog comparator are for DAC testing only.

### 3.1 Testing the AD converter

A typical timing diagram for ADC testing is shown in Fig. 2 (the 1-bit pattern memory stores one period of sawtooth waveform in this example.) To test the AD converter, we first load the pattern memory with the pre-computed one-bit delta-sigma stream, direct the LPF output to the ADC under test, and let the ADC be the input source of the code/index memory. The $gen$ signal is then set to high to activate the signal generation. The $acquire$ signal is set to high when the LPF output enters the useful portion of the sawtooth, which is the part of the linear rising ramp that *covers* the FSR of the ADC, and is set to low when the LPF output leaves the useful portion. The ADC output codes collected when $acquire$ is high are analyzed to derive the Tally and Weight arrays from which the INL and DNL of the ADC can be computed.

Assumes that the duration of the high $acquire$ signal is $l$ clock cycles. With an $n$-bit ADC, the required memory space for storing the ADC output codes is $l$ $n$-bit words. For example, an 8-bit ADC and 4k collected ADC codes needs 4k byte memory space.

### 3.2 Testing the DA converter

When testing the DAC, the pattern memory is loaded with the encoded sawtooth waveform, the LPF output is directed to the analog comparator, and the input source of the code/index memory is the index counter. Also, the pattern counter is loaded with $c_0$ and the index counter is reset. Our DAC BIST scheme uses the linear ramp together with an analog comparator to measure the analog output levels corresponding to each DAC input code. The idea is illustrated in Fig. 3(a). The analog comparator continuously compares the DAC and the LPF outputs. At the beginning of the linear ramp (which covers the DAC's FSR), the former is greater and $positive$ is low. When the value of the linear ramp is greater than $v_0$, the output value corresponding to code $c_0$, the $positive$ signal becomes high. Upon the detection of a rising edge at the $positive$ signal, the controller increments the pattern counter and informs the code/index memory to record the current contents of the index counter, i.e., $t_0$. If

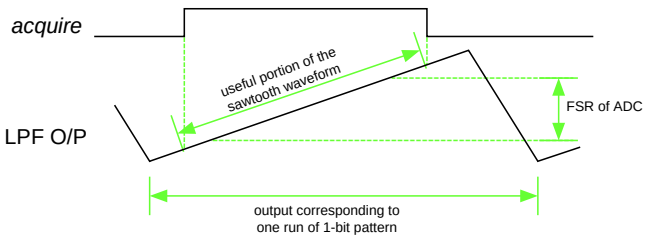


**Figure 2. Timing diagram for ADC testing.**

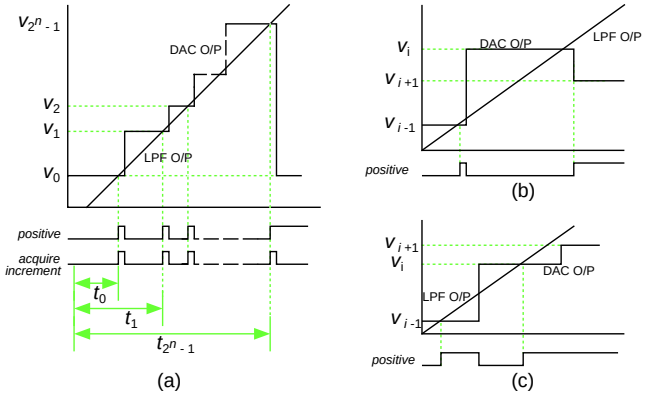


**Figure 3. The DAC testing procedure.**

$v_1$ is sufficiently greater than $v_0$, $positive$ goes down and stays low till the linear ramp reaches $v_1$ when $t_1$ is recorded. If the transfer map of the DAC under test is monotone increasing and the differences between the output levels of adjacent codes are large enough for the analog comparator to generate a rising edge with respect to each input code, one will be able to record $t_i$'s for all the input codes. In such a case, the value of the pattern counter will be $c_0$ and $positive$ is high at the end of the process.

The DAC parameters are computed from the collected indices. First, the average separation between adjacent codes, which corresponds to 1 LSB, is

$$\overline{w} = (t_{2^n-1} - t_0) \,/\, (2^n - 1)$$

One can then compute DNL and INL (as fraction of 1 LSB) by:

$$\begin{aligned} \mathrm{DNL}_i &= (t_i - t_{i-1} - \overline{w}) \,/\overline{w} \\ \mathrm{INL}_i &= \begin{cases} 0 & \text{if } i = 0 \\ \mathrm{INL}_{i-1} + \mathrm{DNL}_i & \text{otherwise} \end{cases} \end{aligned}$$

It can be shown that $\mathrm{INL}_{2^n-1} = 0$ because the approach uses the straight line that passes $c_0$ and $c_{2^n-1}$ as the linearized output line.

In the case when the transfer map of the DAC under test is not monotone increasing, e.g., $v_{i+1} < v_i$ (Fig. 3(b)), or $v_{i+1} - v_i$ is too small (Fig. 3(c)) to have a rising edge at the $positive$ signal corresponding to $c_{i+1}$, the pattern counter's value will be $c_{i+1}$ instead of $c_0$ at the end of the process. To measure $t_j$ for $j \geq i+1$, we restart the process as before except that we don't load the pattern counter (so its value will remain $c_{i+1}$ at the beginning of the process.) The first rising edge at the $positive$ will then correspond to $c_{i+1}$ and $t_{i+1}$ is recorded. As the process continues, $t_j$ for $j > i+1$ will be recorded, too. If necessary, the process may be repeated several times to collect all the $t_i$'s.

The index counter must be able to count up to the length of the useful portion of the rising ramp, $l$, and the memory space for storing the indices is thus $2^n \log_2 l$-bit words. For

example, with an 8-bit DAC and linear ramp of 4k clock cycles, the required memory space is $2^8$ 12-bit words.

### 3.3 The test accuracy

The test strategy for both AD and DA converters is to represent the separation between two analog quantities in terms of the number of occurrences (ADC) or the number of clock cycles (DAC); therefore, quantization error is inevitable. The quantization error can be as large as $2/\overline{w}$ LSB, where $\overline{w}$ is the average code occurrences for ADC testing and the average code output separation for DAC testing. For instance, the quantization error can be as large as 1/8 LSB for $\overline{w} = 16$.

In addition to the inherent quantization error for the linear ramp approach, the noise associated with the generated linear ramp, i.e., its deviation from the ideal straight line, also contributes to the measurement error. Let the RMS value of the deviation be $\varepsilon$, the overall test error is approximately upper bounded by

$$\frac{2}{\overline{w}} + \frac{2\varepsilon}{\mathrm{FSR}/2^n}$$

assuming an $n$-bit converter (the factor 2 reflects the fact that the error can affect the measured values of both sides.)

## 4 Stimulus generation

In this section, we discuss how to generate the linear ramp that achieves the desired measurement accuracy and show that the stimulus quality is tolerant to analog process variation.

The slow-rising linear ramp for testing the converters is a portion of the rising ramp of a sawtooth waveform. Since the sawtooth waveform is a multi-tone signal, the restored waveform at the output of the low-pass filter is distorted (especially at the peaks) because of the missing high-frequency components.

As we have discussed in Section 3.3, the test accuracy is improved as the length of the linear ramp (that maps to the FSR of the converters) increases and the corresponding RMS deviation decreases. In general, one can control (to a certain extent) the length of linear ramp and its RMS deviation by (1) adjusting the depth of the pattern memory, (2) choosing the order and configuration of the delta-sigma modulator for generating the one-bit digital stream, and (3) modifying the shape of the encoded sawtooth wave, i.e., the ratio of the rising ramp to one period. In the following, we will focus on finding the best shape of the sawtooth waveform since the first two are usually constrained by hardware configuration and cannot be adjusted at will.

The configuration of our current setup is as follows: (1) the memory depth of the 1-bit pattern memory is $N = 2^{14}$, (2) the nominal output levels of the 1-bit DAC are $\pm 5$ volts, (3) the FSR for both converters is $\pm 3$ volts, and (4) the resolutions of both converters under test are 8-bit. The desired

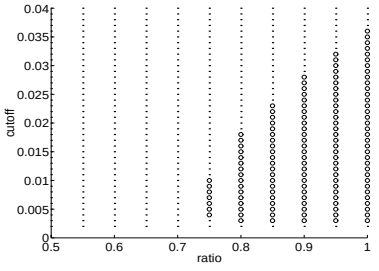


**Figure 4. Finding the best shape of the sawtooth waveform.**

test accuracy is 5% LSB for both AD and DA converters. To maximize the length of the rising ramp in the sawtooth waveform, the 1-bit pattern memory stores exactly one period of a sawtooth waveform. The selection of the software modulator depends on the ratio of the FSR of the converters to the output range of the 1-bit DAC. In general, higher order configurations are preferred if stability is not compromised. For our setup, we use the second-order configuration and set the peak-to-peak value of the sawtooth waveform to be 70% the 1-bit DAC output range. To decide the shape of the sawtooth waveform that maximizes the length of the *usable* linear ramp, we first define the non-linearity associated with a series of evenly sample points $R = r_0, r_1, r_2, \ldots, r_l$ as

$$\varepsilon = \sqrt{\frac{(r_i - (ai + b))^2}{l}}$$

where $l$ is the length of the series, and $y = ai + b$ is $R$'s best-fit line (least square error.) Let $\gamma$ be the ratio of the rising ramp to the period of the sawtooth waveform. We perform a series of simulation that varies the value $\gamma$ from 0.5 to 1 and the cutoff frequency of the 2nd order Butterworth low-pass filter from 0.2% to 4% the output frequency of the 1-bit pattern memory (to evaluate the effect of variation in the low-pass filter.) For each combination of $\gamma$ and cutoff frequency, the test accuracy is computed by

$$\frac{2}{\overline{w}} + \frac{2\epsilon}{\mathrm{FSR}/2^8}$$

where $\overline{w}$ is the length of the linear ramp that maps to the FSR divided by $2^8$, and $\varepsilon$ is the corresponding RMS deviation. Note that the first term represents the quantization error, and the second term the error caused by the non-linearity of the generated linear ramp. The simulation result is shown in Fig. 4. The x and y-axis represent $\gamma$ and cutoff frequency, respectively. Using 5% LSB as the accuracy threshold, each circle/dot represents a configuration that satisfies/fails the desired accuracy. One can see that the desired accuracy is realizable only for $0.7 < \gamma \leq 1$. We choose $\gamma = 1$ for our sawtooth waveform because it is

most immune from the variation in the LPF (with acceptable LPF cutoff frequency ranging from 0.3% to 3.6% the pattern memory clock rate).

Let the nominal output levels of the 1-bit DAC be $\pm b$. At the existence of analog imperfection, the two output levels are perturbed to $b+\delta^+$ and $-b+\delta^-$, respectively. The overall effect is equivalent to multiplying the nominal 1-bit DAC outputs by $m = 1+(\delta^+ - \delta^-)/2b$ followed by the addition of a DC component $c = (\delta^+ - \delta^-)/2$, which theoretically will not affect the linearity of the generated ramp. We use $\gamma = 1$ and cutoff frequency 0.6% the pattern memory output frequency, and perturb both the positive and negative output levels of the 1-bit DAC for up to 4% deviation. Simulation results show that the test accuracy has little variation over the deviations in the DAC output levels—the accuracy ranges from 0.035 LSB to 0.039 LSB (the accuracy for the nominal case is 0.036 LSB.)

From the above simulation, one can see that the stimulus generation scheme is highly tolerant to the analog imperfections in both the 1-bit DAC and the low-pass filter.

## 5 Simulation results

To validate the proposed technique, we perform numerical simulation by applying the generated linear ramp to AD and DA converters with known DNL and INL values. (The setup is as described in Section 4.) From simulation, the length of the useful portion of the linear ramp is 12,781 clock cycles. The required code/index memory space is thus 12,781 8-bit words for ADC testing, and 256 14-bit words for DAC testing.

For ADC testing, Fig. 5(a) and (b) plot the DNL and INL measurement errors using the proposed setup. (The x and y-axis are the code indices and measurement errors as fraction of 1 LSB.) The maximum errors for the computed DNL and INL are 0.049 and 0.038 LSB respectively, which meets our accuracy requirement of 5% LSB.

For DAC testing, the results are shown in Fig. 5(c) and (d), where the measurement errors for DNL and INL are plotted. The maximum errors for DNL and INL testing are 0.042 and 0.046 LSB—both are within the desired accuracy.

## 6 Conclusion

We present a BIST scheme for testing on-chip AD and DA converters. The main advantages are (1) the proposed BIST architecture does not require the existence of both AD and DA converters, which makes it feasible for most mixed-signal IC's, and (2) both the stimulus generation and measurement techniques are highly tolerant to analog variations. We show how the desired test accuracy can be achieved for a given hardware configuration and validate our ideas with numerical simulation results. Our on-going research includes (1) verifying the techniques with hardware setup, and (2) extending the scheme for testing other analog functional blocks.

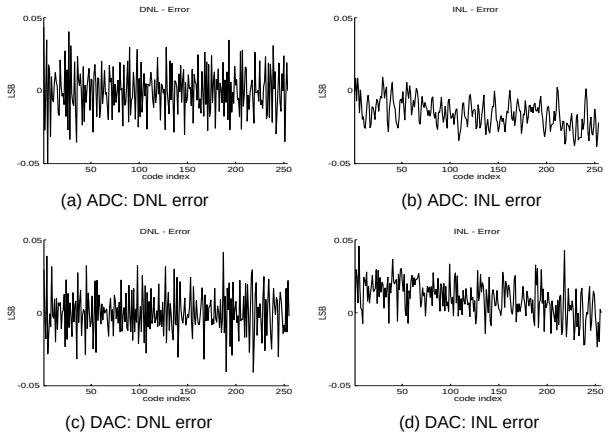


**Figure 5. Simulation results**

## Acknowledgment

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