Test Synthesis for Mixed-Signal SOC Paths*

Sule Ozev, Ismet Bayraktaroglu, and Alex Orailoglu
Computer Science and Engineering Department
University of California, San Diego
La Jolla, CA 92093
{sozev, ibayrakt, alex}@cs.ucsd.edu

Abstract

Higher levels of integration, the need for test re-use, and the mixed-signal nature of today's SOC's necessitate hierarchical test generation and system level test composition to meet stringent market requirements. In this paper, a novel methodology for testing analog and digital components in a signal path is discussed. Consequent testability analysis can be utilized to reduce DFT requirements, while test translation provides highly effective low cost test. The proposed approach seamlessly propagates test information across the analog/digital divide. Experimental results substantiate the effectiveness of the proposed mixed-signal test synthesis methodology.

1. Introduction

Recent developments in semiconductor manufacturing enable integration of highly complex mixed-signal systems on one single chip. While systems-on-a-chip are the only viable solution to the increasingly stringent requirements of the market, they introduce new and challenging circuit test problems. Due to the complexity and mixed-signal nature of today's systems, hierarchical approaches are required for test synthesis. In hierarchical test synthesis, a test set for each module in the system is generated separately. Generated module level tests can be applied through the use of DFT techniques such as scan insertion, test busses and test point insertion. However, as the number of modules in systems increases, the overhead of such costly DFT techniques becomes unpalatable.

Test translation schemes attempt to convert module level tests into system level through the use of existing functional signal paths in the system. In this way, DFT techniques are applied only for tests that can not be translated and performance and hardware overhead can greatly be reduced.

In a mixed-signal SOC, functional signal paths frequently cross the boundary between analog and digital domains. In the context of SOC's, a viable test translation scheme needs to be able to propagate analog signals through digital modules and digital patterns through analog modules. Such propagation schemes require addressing complicated analog-digital interface issues. Resolving analog signal uncertainties, incorporating non-ideal analog behavior, such as noise, clock spurs or non-linearity, while crossing into the digital domain, reconstructing analog signals out of a cluster of digital bits while crossing into the analog domain are examples of such complications. It is also necessary to be able to evaluate test translation in terms of more traditional parameters such as yield and fault coverage.

The most common case of analog to digital signal interface in a mixed-signal SOC is an analog front end connected to a digital filter through an interface module such as an ADC or a $\Sigma\Delta$ modulator. The output of the digital filter usually goes into a signal processing core. The signal path ends at this point since the correlation among signal bits is not preserved in a generic signal processing logic.

Traditionally, tests for analog modules and the digital filter in a signal path are designed separately, without taking system level knowledge into account. On the analog side, these tests are applied through test point insertion. In addition to creating noise and loading interconnects between modules, hence resulting in performance penalty, such a test methodology fails to examine interface and loading issues between analog modules. On the digital side, module level tests are applied through scan insertion or test busses. While both methodologies have large area overhead, scan insertion fails to exercise at-speed test and test busses increase I/O requirements and noise level in the system.

This paper aims at providing an analog-digital interface methodology for testing analog and interface modules and digital filters in a signal path without resorting to expensive DFT methods. Test signals for one module are propagated through other modules in the system. During propagation, signals are modeled with attributes so as to preserve test related information. The models for modules are simple enough to ensure computational effectiveness, but include non-ideal behavior to ensure correctness of test synthesis. The following section serves as an overview of the research activities in the area. Section 3 explains the methodology utilized in test synthesis and section 4 discusses test synthesis in detail. Section 5 presents experimental results on a typical communication system path. The paper concludes with a discussion of experimental results and future research work.

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2. Previous Work

Automation of mixed-signal test generation is still in research phase. As there are no current research efforts specifically aimed at mixed-signal test, we outline in this section efforts in analog test and we briefly describe the state of the art in digital SOC's and functional hierarchical approaches. Until recently, analog test research efforts have focused on test generation at the basic block level. An identification of the effects of manufacturing defects on the output response of the circuit under test using DC input stimuli only is attempted in [4]. Automated generation of test stimuli is the aim of approaches outlined in [7, 6]. These approaches employ output signal sensitivity, a concept introduced in [1], to circuit parameters. In [7, 6], test inputs are defined as single tone sinusoidal signals with frequency as an unknown parameter. The frequency at which the sensitivity of the output voltage (voltage gain) of the circuit is highest to a given component is selected to test it. Evaluation of a given test set by computing determination accuracies of functional parameters is outlined in [1].

In [2], the aim is to derive the pass/fail conditions of basic blocks in a system from the system level pass/fail conditions for DC voltages and currents. The system level requirements at output are back-propagated through a signal path to the output of each basic block in the system. The authors aim at reducing computational complexity by utilizing I/O look-up tables obtained through SPICE simulations.

On the digital front, test generation tools and DFT methodologies have adequately matured so as to be capable of handling system level test generation for moderate size designs. However, the trend towards higher levels of integration by the introduction of core-based design methodologies for SOC's has necessitated increased test reuse. Test reuse is required to reduce time-to-market by cutting down test development as well as to protect core providers by eliminating the need to expose design details. Both industry and the research community, including P1500 standardization efforts [3], have been searching for ways to improve test reuse via test shells at the core level and dedicated or shared test busses at the system level. While functional hierarchical test approaches are developed to overcome test challenges of current designs, most of the research efforts on SOC's, including P1500, have ignored these functional approaches as well as the necessity to provide solutions to the challenging problem of mixed-signal SOC's.

3. Methodology

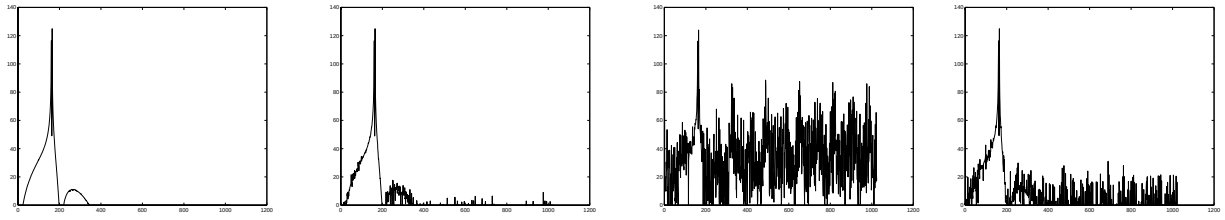
Any signal can be represented as a composition of sine waves at certain frequencies. Even though the shape of the input signal does not effect simulation times for digital circuits, a pure or composite sine signal can be propagated through analog circuits more easily.

The patterns utilized to test the digital filters are propagated to the inputs of the digital circuitry through the analog blocks. Therefore, in order to improve the efficiency of test propagation, we utilize multi-tone sine waves. Structural faults, stuck-at or delay, distort the output waveform, and thus can be detected by observing the distortion in the output signal. Some of these faults manifest themselves as periodic spikes in the waveform, resulting in harmonics in the spectrum. Some faults result in intermodulation products. Figure 1a shows the output response spectrum of the good circuit for a 16-tap filter, when the input is a pure sine wave. A number of plots in Figure 1 show the output spectrum for the same circuit with faults at various locations.

A multi-tone sine wave is capable of detecting a large portion of faults in a digital filter. Fault simulations have shown that even a pure sine wave has a fault coverage of 89.6%. The fault coverage of a two-tone sine wave is 95.5%. Since a two tone sine wave exercises intermodulation faults, it has higher fault coverage. Signals with higher number of tones slightly improve the fault coverage level. Yet the complex and unpredictable behavior of analog circuits for multi-tone signals, under typically used simplified models, precludes their utilization. We therefore in this work utilize signals up to 2-tones. For 2-tone signals, the frequency of both tones needs to be within the pass-band of the filter and the composite amplitude needs to be high enough to exercise a wide dynamic range in order to prevent sign-bit faults from escaping undetected.

The desired sine waves to test digital filters in a signal path can be propagated from primary inputs through analog and interface modules. In the context of mixed-signal test synthesis, one needs to pay attention to distortion in propagated signals due to non-idealities in the analog and interface components. In the analog domain, components create some level of noise and distortion which is tolerable from a system point of view. If the distortion created by a particular fault in the digital filter is below the noise level or it coincides with the distortion generated by an analog component, that fault can not be detected through the propagated signal. In order to compute an accurate fault coverage, such non-ideal components in the signals must be known. Therefore, during propagation of test inputs for a digital filter through mixed-signal components, amplitude and frequency of the signal, as well as noise level and harmonics in the signal must be tracked.

On the analog side, tests are targeted at measuring specified parameters for mixed-signal modules. Some parameter computations require knowledge of only the frequency and amplitude of the input and output signals. Cut-off frequency, 3rd order intercept (IIP_3), and mixer isolation are examples of such parameters. However, some parameters require information about phase and DC level of signals as well as amplitude and frequency. Offset and group delay measurements are examples of such tests. While propagating test signals for a module, the necessary information to compute the parameters needs to be preserved. In addition, noise level and harmonic components in the signal must be



a. Fault-free Response b. Fault in the Multiplier in Tap2 c. Fault in an Adder in Tap5 d. Fault in Tap7 Output

Figure 1. Response:Fault-free and with several Stuck-at Faults

known since they may degenerate test signals.

Another fundamental challenge in mixed-signal test propagation is incorporation of parameter tolerances into test synthesis. The parameters of a defect-free analog module can vary within a range specified by the system designer. As a result, while propagating signals through functional blocks, it is not possible to compute the exact values of certain signal attributes. This indeterminism in signal values produces a corresponding indeterminism in computed parameter values. In some cases, it is possible to adjust the parameter computations through previous system level measurements and decrease the level of uncertainty in computed parameters. Measuring the signal path gain and using this value rather than nominal gain in the computation of the IIP_3 for a module is an example of such an adaptive test strategy. The remaining uncertainty in parameter computation causes some loss in fault and yield coverage. As an example, consider the distribution of a module level parameter, as shown in Figure 2. The parameter has a certain acceptable tolerance, and is considered faulty if it falls outside this tolerance. Uncertainty in computing this parameter may cause either some faulty parts to pass or some good parts to fail the test. In order to ensure correctness of test propagation in the analog domain, the indeterminism in signal attributes needs to be known, and the resulting fault coverage and yield losses need to be computed.

Test response of mixed-signal modules can easily be observed through a digital filter, since the digital filter can be modeled as an analog filter, with cut-off frequency dependent on the digital clock rate, and no added noise or nonlinear distortion.

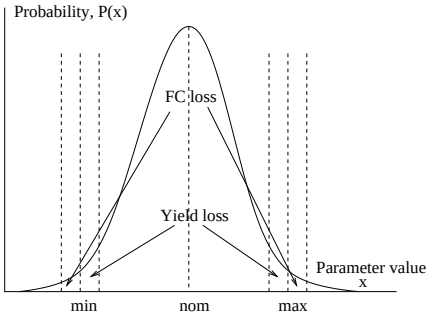


Figure 2. Probability Distribution of a Parameter and its Effect on Fault and Yield Coverage

4. Test Synthesis

Analog and digital domains have distinct requirements for test synthesis for a mixed-signal SOC. Whereas absolute amplitude and frequency of the test signal have insignificant effect on fault coverage, the same signal attributes are used to compute parameters in the analog domain. In this section, important challenges in both domains and proposed solutions are discussed in detail.

4.1. Test for Digital Filters

In current digital test methodologies, simple fault models, approximating defect behavior, are utilized with well defined inputs and expected outputs. Utilization of the functional paths in the analog circuitry in order to propagate the test patterns to the inputs of the digital filter eliminates the precise knowledge of input patterns. While costly DFT solutions, such as observability point insertion may help, a less costly solution is attained by importing methods from the analog domain, such as spectrum analysis. The nonidealities due to gain variance and varying offset of analog circuitry can be eliminated through spectral analysis [5]. However, the perturbations caused by noise and non-linear behavior of analog domain need to be analyzed precisely in order to differentiate these effects from the fault effects due to the digital filter. While the faults with small magnitude effect at the digital filter may be buried in the noise floor generated by the analog circuitry, the non-random behavior of such fault activation events causes fault effects to stand out in the output spectrum.

The level of total noise at the inputs of the digital filter is estimated through spectral analysis of the input patterns [5]. Spectral analysis instead of path analysis is utilized for test of digital filters, since the latter analysis produces higher noise levels. The higher the level of noise estimated, the more will faults with low magnitude be lost. Though in practice the noise may exceed the level of estimated noise, the level may be adjusted by trading off fault coverage loss to yield loss.

4.2. Test for Mixed-Signal Modules

In the analog domain, tests are targeted at measuring parameters specified by the designer. Some of these parameters are direct ramifications of system level requirements. The cut-off frequency and stop-band gain of a filter result

directly from blocking requirements in a communications signal path. Some other parameters result from partitioning a system level parameter. For example, the required gain is partitioned as gains of basic blocks in a signal path. A third group of parameters results from non-idealities in analog components such as 1dB compression point for a mixer, or integral non-linearity (INL) of an ADC. In the context of test translation, these parameter measurements need to be converted to measurements at the system level. In order to enable this conversion, important challenges must be addressed such as modeling signals and basic blocks, computation of system level tests and the effect on yield and fault coverage of measured parameters.

Modeling Signals: During test translation, necessary information needs to be preserved in order to compute circuit parameters. Most parameters are computed from frequency, amplitude, phase, and DC level of the input and output signals. In order to compute parameters that specify noise performance such as dynamic range and signal-to-noise ratio (SNR), the noise level at any point in the system must also be known. Noise level also determines the minimum detectable signal level in the system. Tests that require smaller signal power than noise level may become untranslatable through signal propagation.

Parameters of a defect-free mixed-signal circuit can vary within a range specified by the system designer. As a result, when only primary inputs are controlled and primary outputs are observed, it is not possible to determine the exact values of signal attributes at any point in the system. Such indeterminism in signals introduces a new and challenging controllability problem. Therefore, parameter tolerances and their resultant effects on controllability and observability of basic blocks must be incorporated into a mixed-signal test translation scheme to ensure correctness.

In the proposed test translation scheme, signal propagation is enabled through tracking amplitude, frequency, phase, DC level, noise level, and accuracy of signals as modules are traversed.

Modeling Mixed-Signal Modules: Mixed-signal block models to be utilized in signal propagation have to be as simple as possible to keep the computational cost low, yet accurate enough to ensure correct test translation. To reason about the signals being propagated through basic blocks, the models should include input-output relations, circuit parameters together with their tolerances, and expected non-ideal behaviors such as spurious response or noise figure.

Transfer functions are the most commonly used models for basic blocks for behavioral simulation during the design process. However, as transfer functions model the behavior of the circuit through the complete frequency domain, the resultant representation is quite complex. The proposed scheme utilizes the fact that the behavior of most of the basic blocks used in the design of mixed-signal circuits can be accurately defined with simple terms within some operating range. As an example, consider a switched capacitor low-pass filter (LPF). Although using the transfer function as a model requires complex computations, such as numeric differentiation or integration, a simple linear model can be utilized in the frequency domain if the frequency of operation is below the cut-off frequency of the filter. Moreover, the spurious components in the output waveform due to the clock input can be represented as tones at the integer multiples of the clock frequency.

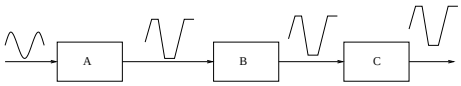


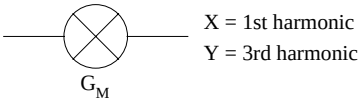
Figure 3. Gain Error Resulting in Saturation

Mixed-Signal Translation Methods: Basic block parameters stem either from direct projections of system level requirements on basic blocks, such as cut-off frequency of a filter, or from partitioning a system level parameter into basic block parameters, such as gain. The tests for the first group need to be conducted separately whereas the tests for partitioned parameters can be composed at the system level. By identifying some of the composable parameters, the proposed scheme utilizes two methods for test translation.

Translation by Composition: Basic block parameters that result from partitioning system level parameters can be viewed as a composed parameter. Dynamic range, gain, and noise figure are common examples of such parameters. In a typical system, the tolerances associated with basic block gains are close in value. In such cases, the individual gains of modules can not be determined with the desired accuracy. However, a composite parameter, the path gain, can be measured with high accuracy. If composed parameters such as path gain are measured, boundary conditions must be checked. Consider a simple system given in Figure 3. The path gain for this system is typically measured around the mid-point of the amplitude operation range. A positive gain error in Block A may be masked by gain deviation of Blocks B and C. However, when a high signal amplitude is applied, the output of Block A may saturate Block B. Such a distortion can not be masked by any other basic block in the path and results in failure. Similarly, a negative gain error in Block A may be masked by gain deviations of Blocks B and C at the mid-point of amplitude operation range. In case of small signal amplitudes, this error may result in signal loss, thus resulting in a system failure.

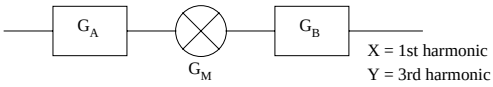
Measurement of SNR at minimum and maximum signal amplitudes is necessary in case the gains of several basic blocks are measured as one composed parameter. In addition to prevention of test point insertion, composition of parameters also decreases the number of required tests in case three or more basic blocks are cascaded.

Translation by Propagation: Some tests are targeted at specific basic block parameters that have no direct or easy-



$$IIP_3 = \frac{3X - Y + G_M}{2}$$

a. IIP_3 computation in case of full access



$$IIP_3 = \frac{3X - Y}{2} - (G_M + G_B)$$

$$IIP_3 = \frac{3X - Y}{2} - G_{path} + G_A$$

b. IIP_3 computation in case of no access

Figure 4. Improving Accuracy

to-extract correspondence at the system level. The third order intercept point of a mixer or the cut-off frequency of a filter are examples of such basic block parameters. In order to test these parameters, required test signals and resultant output responses of corresponding basic blocks must be propagated through other basic blocks in the path.

Improving Accuracy: Inaccuracy in signal attributes results in error in a measured parameter. In some cases, this inaccuracy can greatly be reduced by adjusting parameter computation with respect to previously computed, more accurate parameters.

As an example, consider the IIP_3 measurement for a mixer in a signal path, as in Figure 4. When the measurement is converted to system level, IIP_3 of the mixer is computed through measuring 1st and 3rd order harmonic power at the primary output rather than the output of the mixer. Whereas it is possible to use nominal gains of the mixer and Block B, during the IIP_3 computation, accuracy of this computation will be affected by the gain tolerances both of Block B and of the mixer. It is also possible to compute IIP_3 using the path gain and the gain of Block A. Since path gain is a system level parameter, it can be measured with high accuracy and the computation accuracy of IIP_3 is affected by the gain tolerance of Block A only. Identifying tests that result in less accuracy loss helps in reducing yield and fault coverage losses.

Even though error in parameter computation can be reduced by an adaptive test methodology as described in the previous section, 100% accuracy can not be invariably achieved. This error in parameter computation may cause some good parts to fail the test, which results in yield loss, or some bad parts to pass the test, which results in fault coverage loss. If test synthesis results in unacceptable fault coverage and yield loss, a DFT technique needs to be utilized to decrease the amount of error. Therefore, at the end of test translation, yield loss and fault coverage loss need to be computed to evaluate the design in terms of testability.

Testing a parameter consists of computing the parameter and comparing it against pre-defined bounds. Consider the IIP_3 computation in Figure 4:

$$IIP_3 = \frac{3X - Y}{2} - G_{path} + G_A$$

The test for this parameter consists of comparing it to a minimum value. If the IIP_3 is higher than this minimum, the part passes the test, otherwise it fails the test. The error in this computation stems from the tolerance of G_A. If the actual gain of Block A is lower than the nominal value, some parts with an unacceptable IIP_3 will be accepted as in Figure 5. Similarly if the actual gain of Block A is higher than its nominal gain, some parts with an acceptable IIP_3 will be rejected.

Depending on how strict the specification is, fault coverage loss can be traded off with yield loss by adjusting the minimum required value. If the minimum required value is decreased, yield loss decreases, but fault coverage loss increases. Fault coverage and yield losses are computed using the expected distribution of the parameter and the computation error. Expected distribution of the parameter is either obtained through Monte-Carlo simulations during the design process or predicted from past distributions of similar module parameters implemented with the same process.

5. Experimental Results

The experimental set-up consists of a communications signal path as shown in Figure 6. The incoming signal is amplified and down-converted, and the lower frequency component of the resulting signal is selected by the low-pass filter, which is then digitized by the ADC. The digital filter provides finer channel selectivity.

Tests for mixed-signal modules are designed to measure specified module parameters as listed in Table 1. Gain, dynamic range and noise figure tests are composed at the system level. For parameters that can not be composed at the system level, module level tests need to be converted to system level through signal propagation. In computation of such parameters, some error is encountered due to signal inaccuracies. The adaptive test strategy is utilized by measuring path gain and LO frequency first and using these measurements to decrease error in computation of other module level parameters. The remaining measurement error and resulting fault coverage and yield losses are computed. Test signals are applied at the primary input and test

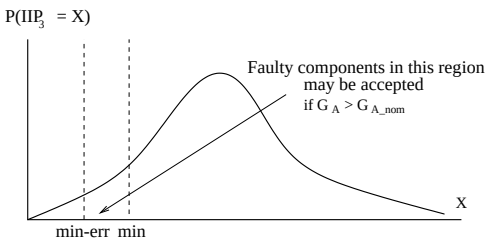


Figure 5. Impact of Error on Fault Detection

Amp	Gain, IIP_3, DC Offset, 3rd Order Harmonic
Mixer	Gain, IIP_3, LO Isolation, NF, 1dB Compression Point ($P1dB$)
LO	Frequency Error, Phase Noise
LPF	$G_{pass-band}, G_{stop-band}, f_c, DR$
ADC	Offset Error, $INL, DNLNF, DR$

Table 1. Set of Parameters to be Tested

	Thr. = Tol		Thr. = Tol-Err		Thr. = Tol+Err	
	FCL	YL	FCL	YL	FCL	YL
$P1dB$	12%	0.8%	0.0%	1.9%	20.0%	0.0%
IIP_3	8.5%	0.6%	0.0%	1.5%	15.0%	0.0%
f_c	6.1%	0.6%	0.0%	1.9%	9.1%	0.0%

Table 2. Fault Coverage and Yield Losses

responses are computed at the digital filter output. Mixed-signal testers digitize analog signals in order to make measurements.

Table 2 shows fault coverage losses (FCL) and yield losses (YL) for various choices of parameter thresholds. If the specification for a parameter is tight, fault coverage loss may not be tolerable. Similarly, if the specification for a parameter is loose, some loss in fault coverage is tolerable. Thus, the threshold may be adjusted such that either yield loss or fault coverage loss is minimal. The specified fault coverage losses are in terms of soft faults, i.e. slight deviations in parameter values. There is no fault coverage loss for catastrophic faults, as measurements with slight errors are still capable of detecting large deviations in parameter values. Therefore, the actual fault coverage is higher when catastrophic faults are considered.

The 13-tap low pass digital filter is tested through a two-tone sine wave, which is propagated through the analog circuitry. While an ideal two-tone sine wave is utilized during good circuit simulations, a realistic model of the analog blocks, including varying noise, INL, and offset, is utilized during faulty circuit simulations.

The level of uncertainty at the outputs is determined through spectral analysis. The faulty circuit behavior for each of the faults in the filter implementation is simulated and an output spectrum is generated for each of the faults. The level of output uncertainty is observed to be higher near the applied sine wave frequencies. Therefore, the output spectrum of the good circuit behavior is compared to the faulty circuit spectrum within a tolerance, for the frequencies where the uncertainty level is uniform.

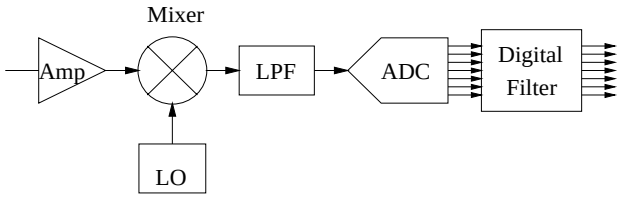


Figure 6. Experimental Set-Up

The results indicate that the fault coverage for the 2-tone input signal, assuming that the exact inputs to the filter are known, is 95.5%. When noise and non-linearity from analog components are incorporated, the spurious-free dynamic range (SFDR) of the filter input signal is 62dB, and SNR is 70dB. Spectral analysis of fault simulations provides a coverage level of 80.1% for 4096 patterns. Analysis of the remaining faults list verifies that undetected faults are scattered within the 5 least significant bits, accounting for a perturbation of less than 1% at the output. The novel fault simulation method for the digital filter is repeated with 8192 patterns for the remaining faults. 7.1% of the remaining faults are detected to increase the fault coverage level to 81.4%. The increased number of patterns magnifies the effect of the fault at specific frequencies as a periodic input signal produces a periodic fault activation.

6. Conclusion

The increasingly important problem of testing Systems-on-Chip with mixed analog/digital components requires cost effective answers. In this paper, we propose a methodology that enables the generation and propagation of test seamlessly across the analog/digital divide. Not only is the necessity for a large number of test points for analog test thus obviated but furthermore no specific test generation hardware is necessary for digital test. The proposed approach is substantiated through an application to a mixed-signal communication chip, which shows a precipitous reduction in DFT requirements for the analog part and high fault coverages in the digital side for faults above the system noise level.

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