Stay Away from Minimum Design-Rule Values

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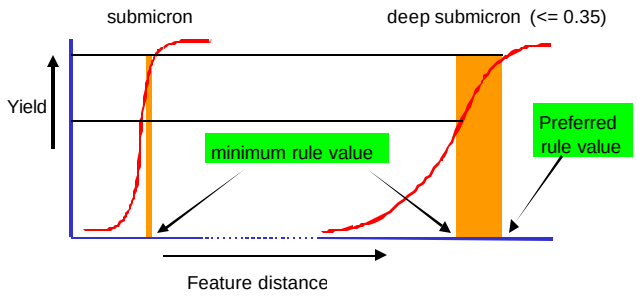
1. Introduction

With the introduction of 0.18 micron CMOS process technology a new phenomenon in circuit manufacturing can be observed: design-rule values as specified in the design-rule manual are no longer “hard” numbers. Where designers and EDA tool manufacturers used to consider rule-values as strict limits when creating mask layouts, rule values have turned into gray areas around the specified rule values. This concept is illustrated in the following figure:



In the case of an UDSM process, the choice of a design-rule value is somewhere in the high-end of the yield range. Choosing a larger value guarantees a higher yield for a particular rule, but results in less dense designs. A lower rule-value implies the opposite: manufacturing-yield will be less, but designs are denser.

These preferred values and types of rules are not a novel concept by themselves. The new thing with UDSM processes is that the preferred values are being defined for common spacing and width rules.

Many foundries specify together with the minimum allowed rule-value also a so-called preferred design-rule value. If preferred values are used wherever space permits in the final layout, a substantially higher manufacturing yield can be obtained.

2. Avoid using minimum rule values

A necessary design paradigm in design for manufacturability in UDSM processes therefore is to avoid implementing minimum design-rule values wherever possible. Only where design-density is at stake, the minimum allowed design-rule values should be used. Only along the so-called critical path that determines the dimensions of a block the drawback on yield will pay-off against using larger rule values. Using larger rule-values on the critical path will result in larger silicon area of the design, which leads to higher cost of silicon and reduced yield because of larger die-size.

On all locations that are not dimension-critical in the final mask layout, larger than minimum rule-values should be respected. If implemented properly and consequently, a defect falling randomly on the wafer during fabrication simply has a lesser chance of introducing a fatal circuit malfunction. In addition, mask-layout post processing before manufacturing, such as optical proximity correction and the use of phase shifting masks will be facilitated.

Introducing non-minimum rule-values in the design is not something that can be implemented by the foundry after tapeout. For that, the consequences on design performance and functionality are too large. The implementation of preferred rules will have to be an integral part of the design flow for enhanced manufacturability. Only then the designer is able to fully verify the final design, including the consequences of for example using a wire-spreading tool on the final routing of the standard-cell blocks.

3. Where can EDA tools help?

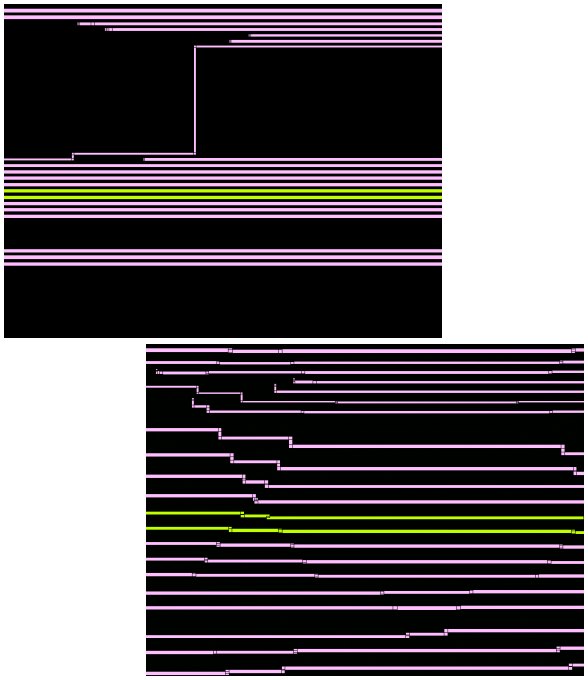
It is obvious that automation is needed to implement larger than minimum design-rule values effectively and efficiently. If we add to the complexity of the problem the fact that certain preferred rule values are more preferred than others – because of the difference in yield-gain – it becomes clear that a manual approach to the problem is doomed to produce a sub-optimal result. In addition it will be consuming too much precious human resources.

EDA tools for implementing non-minimum rule-values should assist designers in the following areas:

- Routing
- Design of custom-cells
- Definition of design-rule values
- Verification for DfM

3.1. Routing

When routing a design, the distances between adjacent wires should be made non-minimum wherever possible. When constructing the routing this is not feasible: if at that stage non-minimum rules would be used, many signals would end up being unconnected. Instead, a postprocessing on the routed design has to be run, known as wire spreading. An example of wire spreading is in the following figure:



Not only is an implementation of wire spreading as shown of great benefit to manufacturing yield, the reduction cross-capacitance is also beneficial to design-performance and power consumption and it reduces the risk of crosstalk between adjacent signals.

3.2. Design of custom cells

Custom cell creation is still very much dominated by manual layout design, be it for standard-cells or regular blocks like memories. Again, introducing non-minimum spacing while drawing the layout is a highly complex task. Designers will be facing a high risk of having to “create space” to get that cell to fit it’s required footprint. That positions the introduction of non-minimum rules in a custom cell layout to be a postprocessing task following full-custom layout design. Designers, instead, should focus on what they’re good at: creating the densest possible cell layout. The enhancement of the layout to ensure better manufacturing yield can be automated by using layout compaction software.

A layout compactor is able to reposition each individual polygon edge in order to produce a design-rule correct design. In addition, the layout can be optimized for performance reducing lengths of wires and the use of high-capacitance layers. Optimization for yield is done by an analysis of the layout for the available “slack” at each polygon edge, followed by distributing that slack over the locations where it returns the most manufacturing yield. To that purpose each preferred rule value can have its own DfM priority.

3.3. Definition of design-rule values

When designing a new process, it’s up to the process engineer to pick a suitable number in the manufacturability range measured for each rule. A full evaluation of the consequences of choosing a particular set of rule-values is a far from trivial task; it essentially requires the construction of test-designs that use the proposed rules in the most optimal way. Layout compaction software can help in this respect by being able to quickly implement a set of new minimum (and preferred!) design-rule values on a collection of given test designs. This allows a proper tradeoff between manufacturing yield and design density to be made already in the process definition stage.

3.4. Design verification

The last stage requiring EDA tool assistance is that of design verification. Needed is, next to a DRC and LVS reports, a manufacturability analysis of a particular cell that highlights the hot spots for yield. Ideally, locations should be flagged where minimum rule values are used without necessity.

4. Conclusion

The use of non-minimum design-rule values will be an important aspect of design for manufacturability in future UDSM processes. EDA tools can and must assist in realizing appropriate design flows. Wire spreading and layout compaction tools are available today to implement preferred design-rule values on mask-layouts for enhanced manufacturability. The area of verification for manufacturability needs to be explored in the near future.