Yield Improvement and Repair Trade-Off For Large Embedded Memories

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Abstract

In this paper, we give an overview of the trade-off to improve yield and optimize silicon manufacturing cost. The specific technology focus is on large embedded memories in complex ASIC or system-on-chip designs. Embedded capabilities for test, redundancy analysis and repair are shown as design-for-manufacturability features needed for large embedded memories in VDSM design.

Keywords: Yield improvement, DFM, BIST, silicon repair

1 Introduction

The degree of manufacturing success is measured by yield, which is defined as the average ratio of the number of usable chips that pass manufacturing test to the total number of potentially usable chips. A way to improve yield is by reducing defect occurrences. The defects produced during the manufacturing process can be eliminated by introducing capabilities to bypass the defects by swapping in redundancies. This can significantly enhance the yield of the manufacturing process, improve reliability of the outgoing product, and increase quality of overall system.

The traditional approach to memory placement in electronic systems has been to embed small memories mostly on logic chips with the much larger main memories implemented in stand-alone commodity memory chips. While this approach in principle continues to exist, but recent advancements in semiconductor process technology provide the ability to build complex and dense memories and to embed them in large ASIC or system-on-chip (SOC). Today's large embedded static/dynamic RAMs and flash memories are cases in point. They typically can store up to 256M bits in 0.18 micron technology.

2 Yield Limitations

The continuous advancements in semiconductor process technology are not without limitations. In particular, these large embedded memories in combination with the process limitations can result in poor overall yield. Depending on the application and design, much of the yield loss can be attributed to defects in the large embedded memories. In order to circumvent this problem, semiconductor manufacturers started to add redundancy into their large embedded memories to perform repair after manufacturing. The redundancy appears in spare rows and/or columns of memory cells to contribute to the repair process if defective cells are detected. This is typically practiced for memories beyond certain sizes depending on the process maturity.

For many years now, redundancy-based repair has been performed regularly during the manufacturing of commodity stand-alone memories. The test for a stand-alone memory is typically performed by a dedicated memory test system, which produces the failed bit map for a defective memory under test. The failed bit map file is transferred to a redundancy analysis station after which the memory reconfiguration is performed by a fuse-blow process using laser repair equipment.

3 Test and Repair for Embedded Memories

The chips that contain large embedded memories today's typically comprise other heterogeneous types of circuits, such as digital logic, and analog block on the same chip. Different circuit types exhibit distinct defect behavior and call for distinct testing and repair. In a conventional test model, each circuit type requires dedicated external test equipment - one tester for logic testing, another for embedded memories test and acquisition of failed bit map data, and yet another for analog test. The use of multiple external testers for a single chip is known as multiple insertion and is held to be an expensive proposition. An alternative solution preferred by test equipment vendors is to use super functional testers, often called SOC testers, which include the test and diagnostic features listed above for all three circuit types. But again this solution is extremely expensive. Because super functional testers do not assume embedded test capabilities in the chip, hence they tend to contain all test features. For instance, a super

functional tester needs, in addition to digital logic test features, to contain options that allow automatic program generation (APG) for memory testing and large capture memory to store the failed bit map data. In such a conventional test/repair practice, the redundancy analysis and laser repair stages are similar to the standalone memory test. The post repair go/nogo test stage requires a tester with APG option for memory retest. As chips continue to grow in complexity, this solution becomes extremely expensive, not only in equipment capital and operation, but also in silicon cost. The silicon factor is mainly due to the high bandwidth and direct test access mechanism (test highway) required on-chip to access and perform the memory test from/to the functional tester.

4 BIST in Test/Repair of Embedded Memories

The need to add an APG option to test embedded memories using functional testers and the need to create increasingly wide on-chip test access mechanisms to access the embedded memories, have resulted in the wide acceptance of Built-In Self-Test (BIST). BIST embeds the memory test function on-chip. The functionality of a BIST block is equivalent to the on-chip test access mechanism and the APG required to test the embedded memory.

The presence of embedded test to perform BIST on-chip removes the need for a wide test highway on-chip, and also removes the need to add APG option to a tester. This turns the functional tester into a low cost tester without memory APG. Today, the memory BIST IP is commonly used in the embedded memory design process. In addition to all cost related benefits, BIST also allows at-speed test of the embedded memories. This has become a critical need for chips operating beyond a certain frequency level.

The use of BIST does not impact the memory redundancy analysis and laser repair processes. However, it positively impacts the post repair tester. Since with BIST, this tester can be simplified. Again a low cost tester without memory APG requirements becomes sufficient, because the memory test function has turned to an embedded test capability that can be reused at this, and any other subsequent, test stage.

5 Built-In Redundancy Analysis

As the complexity of embedded memories keep growing several new challenges appear on the scene of embedded memory test and repair. One of these challenges is the bandwidth limitation of the full failed bit map acquisition required for Redundancy Analysis, from the chip. The limitation of the bandwidth is due to the fact that the memory content has become extremely large and the discrepancy between the speed of the embedded test block (BIST) and the speed of the Logic Tester kept growing. While BIST runs the embedded memory test at-speed, the bandwidth limitation increases the difficulties in transferring the acquired bit map to the External Tester. In addition to the bandwidth problem, the memory capture required to store the failed bit map on the External Tester is growing continuously and becoming very expensive.

The Built-In Redundancy Analysis (BIRA) capability addresses the above two challenges (bandwidth discrepancy and large memory capture). Instead of transferring the full fail bit map data to the external world for analysis. BIRA extends the role of the embedded test and repair function, which was introduced as BIST-only in the previous section, to allow on the fly diagnosis of the failed bits and real time analysis of its results based on the embedded memory redundancy availability and the spare cell allocation algorithm. As a result of the analysis, the BIRA function identifies the actual rows and/or columns in need of reconfiguration. In this case, only the redundancy configuration map is communicated to the external tester. This map is much smaller compared to the actual failed bit data. Hence, it reduces the impact of bandwidth limitation on the test process and removes the expensive memory storage requirement on the external tester. Here the low cost tester is simplified further in terms of memory storage requirements, and the external redundancy analysis stage is removed. In addition, there are the benefits of improving the efficiency of overall test and repair and reducing the time required to perform the redundancy analysis process.

6 Built-In Self-Repair for Embedded Memories

Laser repair is becoming increasingly expensive and is requiring dedicated expertise. Most SOC manufacturers incorporating complex embedded memories on-chip are not manufacturers of commodity memories. Hence they probably do not have the equipment and expertise required for laser repair. As the embedded test and repair functions become more elaborate and self-contained, the natural extension of BIRA becomes the in-situ repair of the embedded memory. Hence, there is no need for repair map transfer and neither the use of laser repair equipment and processes. But rather, the fuse based hard repair turns into soft repair, namely Built-In Self-Repair (BISR). In addition to BIST and BIRA, BISR includes the storage of repair data and controls the soft reconfiguration mechanisms. Embedded test and repair function, which performs BISR introduces the ultimate intelligence on-chip and drastically simplifies the test and repair processes of chips with complex embedded memories. The simplified test and repair process where the low bandwidth communication between

the chip and the tester can be handled either by the Logic Tester used in the case of BISR based approach.

7 Conclusions

In summary, embedded test and repair technology for large embedded memories today has moved beyond fault detection to include effective failed-bit diagnosis, redundancy analysis, and self-repair.